W65C02SOL-28 Microcontroller Datasheet

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DOCUMENT REVISION HISTORY

Version	Date	Authors	Description
1.0	11/16/2021	Bill Mensch, David Gray	Initial Document Entry

1 INTRODUCTION

The W65C02SOL-28 Microcontroller Datasheet is for The VLSI MPW SOL Design Class for use with the Muse Semiconductor MPW services with the PragmatIC FlexLogIC 3u process node.

This datasheet includes information for the W65C02SOL-28 System-on-a-Label (SOL). Separate datasheets are available for the W65C02SOL-28M08SA Intel MAX10M08SA FPGA Microcontroller for emulation of the SOL ASIC and the W65C02SOL-28TEB Test and Evaluation Board.

MyMENSCH™ Rev-C uses a W65C51RTL to drive the CH340 serial-to-USB code port interface for use with WDCTools for both Assembly and C language code development.

The microprocessor unit (MPU) is the W65C02RTL microprocessor. The WDC65xx microcontrollers have interfaces for connected Things for sensing, processing, communicating and actuating (SPCA) are described with the Verilog HDL for use with both FPGAs and ASIC design and manufacturing flow.

This product description assumes that the reader is familiar with the W65C02S 8-bit CPU family hardware and programming capabilities. Refer to documentation on the WDC65xx.com website, ***Programming the 65816 Including the 6502, 65C02 and 65802*** Manual,

1.1 Key Features of the W65C02SOL-20 Microcontroller

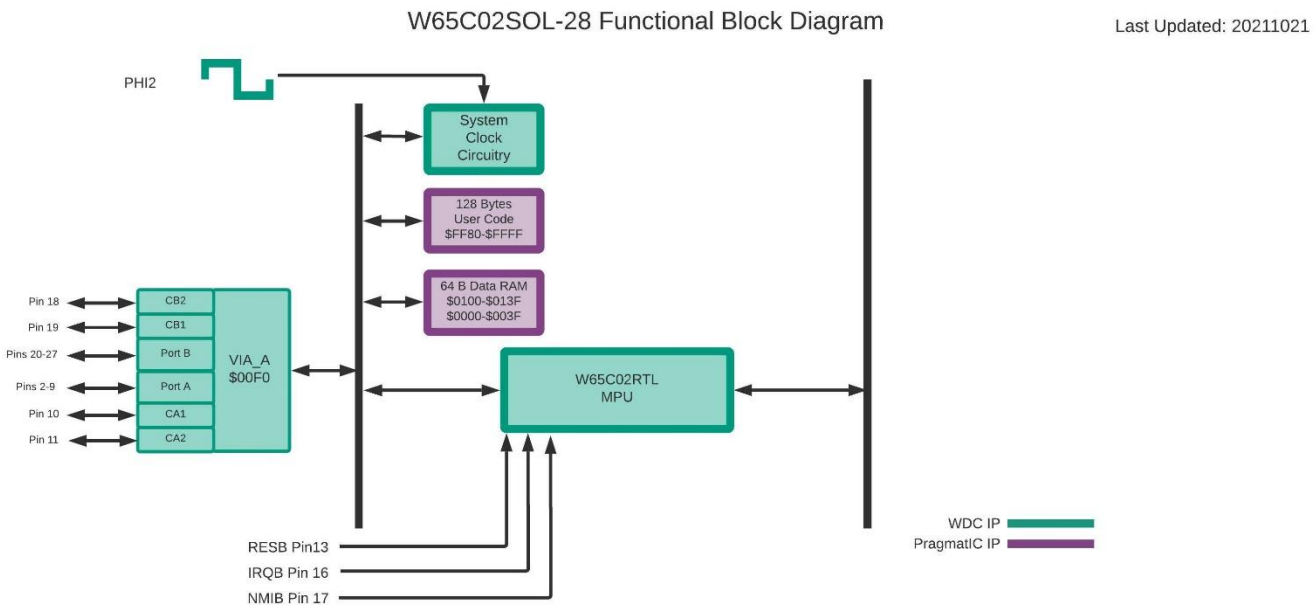
- Operating Voltage – TBD
- System Operation Speed – Determined by the chosen Oscillator
- W65C02RTL MPU
- W65C22RTL VIA
- 1kb (128 Bytes) User code space Hard Mask Programable at MT2
- 512b (64 Bytes) of SRAM in Page 0/1

1.2 W65C02SOL-20 Pin Function List for 28 Pin PDIP/CDIP

- 2x VDD
- 2x VSS
- PHI2 system clock
- RESB REStart
- NMIB Non-Maskable Interrupt
- IRQB Interrupt
- 20x VIA_A

1.3 Functional Block Diagram

The following block diagram is for the W65C02SOL-20.



2 MODULE DESCRIPTIONS

Following are descriptions of the basic modules.

2.1 CLOCK MODULE

There is one main PHI2 system clock..

2.2 RESET MODULE

There are no Reset Module Registers and therefore no definitions. This is a basic module to handle the reset aka restart logic for the system.

2.3 W65C02RTL Programming Model

Refer to the W65C02S Datasheet for the Microprocessor Programming Model, Status Register Coding and complete information. More information is found in ***Programming the 65816: Including the 6502, 65C02 and 65802*** Manual available through Amazon.

2.4 Interrupt Information

The Interrupt Control Module controls the priority and memory map for interrupts.

Vector Address	Label	Function
0xFFFE,F	IRQBRK	BRK – Software Interrupt
0xFFFC,D	IRQRES	RES – "REStart" Interrupt
0xFFFA,B	IRQNMI	Non-Maskable Interrupt

2.5 Memory Map

Start	End	Size	Description
0xFF80	0xFFFF	128 B	128 Byte User Code
0x00F0	0x00FF	16 B	VIA_A
0x0(000x)00	0x0(000x)3F	64 B	64 Byte SRAM

2.6 VIA Port Module

The W65C02SOL-20 features one Versatile Interface Adapters (VIA) based on the W65C22S. See Memory Map for base addresses. See W65C22S Datasheet for full register descriptions.

3 IO Connectors with Ball Assignments on MyMENSCH™ Rev-C

3.0 Left IO Connector J3 on MyMENSCH™

The J3 left connector has 46 IO, 2x 3v3 power and 2x VSS pins. Ball assignments labeled NA are Non-Assigned pins.

J3 – Left Expansion Connector					
Pin	***Signal Name***	***FPGA Ball***	***Pin***	***Signal Name***	***FPGA Ball***
1	VSS	-	2	VDD	-
3	NA	L4	4	NA	L3
5	NA	K6	6	NA	K5
7	NA	H4	8	NA	N2
9	VIA_A_CB2	M4	10	NA	N3
11	VIA_A_CB1	M5	12	NA	N4
13	VIA_A_PB7	L5	14	NA	N5
15	VIA_A_PB6	N7	16	NA	N6
17	VIA_A_PB5	N8	18	NA	M7
19	VIA_A_PB4	M9	20	NA	M8
21	VIA_A_PB3	M10	22	NA	N9
23	VIA_A_PB2	M11	24	NA	N10
25	VIA_A_PB1	N12	26	NA	N11
27	VIA_A_PB0	M13	28	NA	M12
29	VIA_A_PA7	L13	30	NA	L12
31	VIA_A_PA6	K13	32	NA	K12
33	VIA_A_PA5	K8	34	NA	J8
35	VIA_A_PA4	J9	36	NA	L10
37	VIA_A_PA3	K10	38	NA	L11
39	VIA_A_PA2	K11	40	NA	J10
41	VIA_A_PA1	H9	42	NA	H10
43	VIA_A_PA0	J12	44	NA	J13
45	VIA_A_CA1	H13	46	NA	G12
47	VIA_A_CA2	G13	48	NA	F12
49	VDD	-	50	VSS	-

3.1 Right IO Connector J4 on MyMENSCH™

The J4 right connector has 46 IO, 2x 3v3 power and 2x VSS pins. Ball assignments labeled NA are Non-Assigned pins. The ADC inputs are not used for this build and should not be connected to anything.

J4 – Right Expansion Connector					
Pin	***Signal Name***	***FPGA Ball***	***Pin***	***Signal Name***	***FPGA Ball***
1	VDD	-	2	VSS	-
3	NA	H3	4	AGND	(G2)
5	NA	H1	6	ADC_IN0	(F5)
7	NA	H2	8	3v3REF	(F6)
9	DNU/ADC_IN5	F1	10	5vBAT	(G1)
11	DNU/ADC_IN6	E1	12	NA	(E5)
13	DNU/ADC_IN7	C1	14	DNU/ADC_IN1	D1
15	DNU/ADC_IN8	B1	16	DNU/ADC_IN2	C2
17	NA	B2	18	DNU/ADC_IN3	E3
19	NA	A2	20	DNU/ADC_IN4	E4
21	NA	B3	22	NA	E6
23	NA	B4	24	NA	A3
25	NA	B5	26	NA	A4
27	NA	B6	28	NA	A5
29	NA	B7	30	NA	A6
31	NA	A7	32	NA	D9
33	NA	A8	34	NA	E8
35	NA	C9	36	NA	F8
37	NA	C10	38	NA	A9
39	NA	B10	40	NA	A10
41	NA	B11	42	NA	A11
43	NA	B12	44	NA	A12
45	NA	B13	46	NA	C11
47	NA	C13	48	NA	C12
49	VSS	-	50	VDD	-

4 W65C02SOL-20TEB Description

4.1 DIP Socket on W65C02SOL-20TEB

U1 – W65C02SOL-20TEB DIP Socket			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	VSS	28	VDD
2	PA0	27	PB0
3	PA1	26	PB1
4	PA2	25	PB2
5	PA3	24	PB3
6	PA4	23	PB4
7	PA5	22	PB5
8	PA6	21	PB6
9	PA7	20	PB7
10	VDD	19	VSS
11	CA2	18	CB2
12	PHI2	17	NMIB
13	RESB	16	IRQB
14	VDD	15	VSS

5 FCC Compliance

The Western Design Center, Inc. (WDC) provides the enclosed product under the following conditions: This board is intended for use for Education, Engineering Development or Evaluation Purposes ONLY and is not considered by WDC to be a finished consumer product. This board should be handled with caution using good electronics handling practices. This board is compliant per RoHS/Green directives. It does not fall within the scope of directives such as FCC, CE, and UL. It generates uses and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules.

6 Ordering Information

The W65C02SOL-28TEB are available from WDC as part of the W65C02SOL-28 VLSI SOC Design Course.