W65C02SOC-40 Microcontroller Datasheet

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DOCUMENT REVISION HISTORY

Version	Date	Authors	Description
1.0	09/01/2021	Bill Mensch, David Gray	Initial Document Entry
1.0	09/28/2021	Bill Mensch, David Gray	Reduced to W65C02RTL, W65C22RTL, SRAM, Monitor ROM
1.0	10/01/2021	Bill Mensch, David Gray	Removed the Qwiic, Grove add VIA, User and USB connectors
1.0	10/02/2021	Bill Mensch, David Gray	Updated with text changes and connector descriptions.
1.0	10/12/2021	Bill Mensch	Updated text
1.0	10/15/2021	Bill Mensch, David Gray	Added I2C, SPI, UART, etc. Changed name to W65C02SOC-40
1.0	10/19/2021	David Gray, Bill Mensch	Corrected signal pinout for XCLK and SCLK
1.0	11/17/2021	David Gray	Added Board Diagrams for EDU and TEB

1 INTRODUCTION

The W65C02SOC-40 Microcontroller Datasheet is for The VLSI MPW SOC Design Class for use with the Muse Semiconductor MPW services with the TSMC 180nm process node.

This datasheet includes information for the W65C02SOC-40 System-on Chip (SOC), W65C02SOC-40M08SA Intel MAX10M08SA FPGA Microcontroller for emulation of the SOC ASIC and the W65C02SOC-40TEB Test and Evaluation Board.

MyMENSCH™ Rev-C uses a W65C51RTL to drive the CH340 serial-to-USB code port interface for use with WDCTools for both Assembly and C language code development.

The microprocessor unit (MPU) is the W65C02RTL microprocessor. The WDC65xx microcontrollers have interfaces for connected Things for sensing, processing, communicating and actuating (SPCA) are described with the Verilog HDL for use with both FPGAs and ASIC design and manufacturing flow.

This product description assumes that the reader is familiar with the W65C02S 8-bit CPU family hardware and programming capabilities. Refer to documentation on the WDC65xx.com website, ***Programming the 65816 Including the 6502, 65C02 and 65802*** Manual,

1.1 Key Features of the W65C02SOC-40 Microcontroller

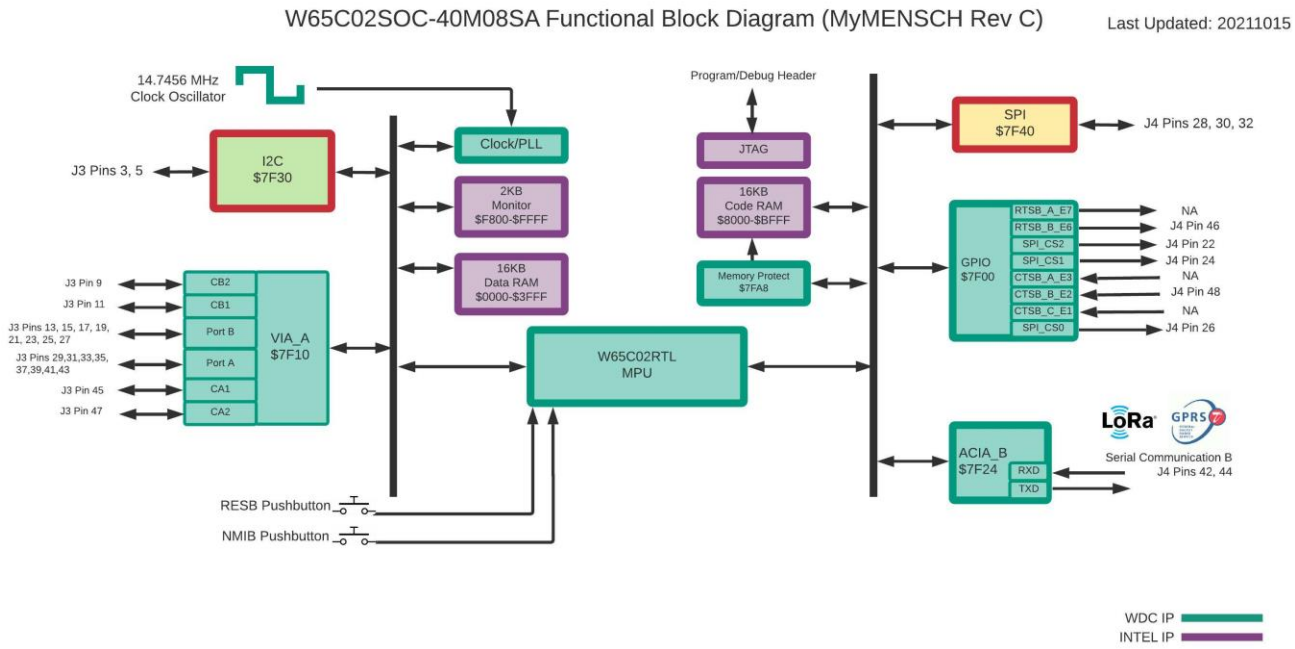
- IO Operating Voltage – 3.3V
- Core Operating Voltage – 1.8V
- System Operation Speed – Determined by the chosen Oscillator
- W65C02RTL MPU
- W65C22RTL VIA
- W65C51RTL ACIA (x2) – XTLI @ 1.8432 MHz
- W65CGPIO ports (8 pins per port) (x4 ports)
- SPI Primary
- I2C Primary
- WDC 2K byte Monitor for boot loading and debugging code
- 16K bytes User code SRAM boot loaded from USB or copied from external SPI serial FLASH memory
- 16K bytes for for data SRAM
- JTAG available on MyMENSCH™

1.2 W65C02SOC-40 Pin Function List for 40 Pin PDIP/CDIP

- 1x 3v3 VDD
- 1x 1v8 Core VDD
- 2x VSS
- 20x VIA_A
- 4x ACIA_A with Handshake (on GPIO)
- 4x ACIA_B with Handshake (on GPIO)
- 2x I2C
- 4x SPI
- 2x SCLK (Serial UART CLK), XCLK (System CLK)

1.3 Functional Block Diagram

The following block diagram is for the W65C02SOC-40.



2 MODULE DESCRIPTIONS

Following are descriptions of the basic modules.

2.1 CLOCK MODULE

There is one main system clock (XCLK) aka PHI2. The Serial UART clock (SCLK) is for the UART baud rate.

2.2 RESET MODULE

There are no Reset Module Registers and therefore no definitions. This is a basic module to handle the reset logic for the system.

2.3 W65C02RTL Programming Model

Refer to the W65C02S Datasheet for the Microprocessor Programming Model, Status Register Coding and complete information. More information is found in ***Programming the 65816: Including the 6502, 65C02 and 65802*** Manual available through Amazon.

2.4 Priority Interrupt Controller Module Information

The Interrupt Control Module controls the priority and memory map for interrupts. Each interrupt is connected to the Interrupt Control Module for prioritizing.

Interrupt Enable Registers for the various interrupts are the interrupt enable by the various enable bits. Reading the various IER and IFR bits determines the interrupt that occurred. By prioritizing the interrupts one can determine which interrupt occurred in the associated interrupt handler routine. Notice that any of the 8 interrupts for a GPIO 8-bit port will cause a GPIO vectored interrupt to occur.

2.4.1 Priority Encoded Interrupt Vector Module

Vector Address	Label	Function
0xFFFE,F	IRQBRK	BRK – Software Interrupt
0xFFFC,D	IRQRES	RES – "REStart" Interrupt
0xFFFA,B	IRQNMI	Non-Maskable Interrupt/Hardware Breakpoint (HBP)
0xFFF8,9	IRQGPIO_HS	GPIO Interrupt for UART Handshaking (for all 8 pins)
0xFFF6,7	IRQVIA_A	VIA Interrupt
0xFFF4,5	IRQSPI	SPI Interrupt
0xFFF2,3	IRQI2C	I2C Interrupt
0xFFF0,1	Reserved	Reserved

2.5 Memory Map

Start	End	Size	Description
0xF800	0xFFFF	2048 B	2048 Byte Monitor
0x8000	0xBFFF	16384 B	16K Byte Protected Bootloaded RAM
0x7FA8		1 B	Memory Protect
0x7F40	0x7F45	6 B	SPI
0x7F30	0x7F35	6 B	I2C
0x7F24	0x7F27	4 B	ACIA_B
0x7F20	0x7F23	4 B	ACIA_A
0x7F10	0x7F1F	16 B	VIA_A
0x7F00	0x7F04	5 B	GPIO – UART Handshaking
0x0000	0x3FFF	16384 B	16K Byte SRAM

2.6 VIA Port Module

The W65C02SOC-40 features one Versatile Interface Adapters (VIA) based on the W65C22S.
See Memory Map for base addresses. See W65C22S Datasheet for full register descriptions.

2.7 GPIO Port Modules

One GPIO Port Module is included on this design. This 5 Register (8-bit) version supports edge sense interrupts and has a PIO Register (PIOx), Data Direction Register (DDRx), Interrupt Flag Register (IFRx), Interrupt Enable Register (IERx), and Edge Sense Register (ESRx). This GPIO is intended to be used as handshake logic for the 2 ACIA modules and Chip Select Outputs for SPI. See Memory Map for base addresses.

2.7.1 GPIO Module Register Descriptions - 5 Register Version

Address = Base + 4		GPIO_ESR: GPIO Edge Sense Register					Reset Value = 0x00	
7:0->	ESR7	ESR6	ESR5	ESR4	ESR3	ESR2	ESR1	ESR0
Bit	Name	Access	Description					
7 – 0	ESR[7:0]	R/W	1 = Positive Edge Sense for PIO7-0					
			0 = Negative Edge Sense for PIO7-0					

Address = Base + 3		GPIO_IER: GPIO Interrupt Enable Register					Reset Value = 0x00	
7:0->	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
Bit	Name	Access	Description					
7 – 0	IER[7:0]	R/W	1 = Enable Interrupt on inputs for PIO7-0					
			0 = Disable Interrupts on inputs for PIO7-0					

Address = Base + 2		GPIO_IFR: GPIO Interrupt Flag Register					Reset Value = 0x00	
7:0->	IFR7	IFR6	IFR5	IFR4	IFR3	IFR2	IFR1	IFR0
Bit	Name	Access	Description					
7 – 0	IFR[7:0]	R/W	1 = Interrupt Occurred on inputs for PIO7-0					
			0 = Interrupts did not occur on inputs for PIO7-0					

Address = Base + 1		GPIO_DDR: GPIO Data Direction Register					Reset Value = 0x00	
7:0->	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
Bit	Name	Access	Description					
7 – 0	DDR[7:0]	R/W	1 = PIO data direction set to Output PIO7-0					
			0 = PIO data direction set to Input PIO7-0					

Address = Base		GPIO_DATA: GPIO Data Register					Reset Value = 0x00	
7:0->	PIO7	PIO6	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0
Bit	Name	Access	Description					
7 – 0	PIO[7:0]	R/W	1 = PIO line is logic 1 value read and sets a 1 value on write for PIO7-0					
			0 = PIO line is logic 0 value read and sets a 0 value on write for PIO7-0					

2.8 ACIA Modules

The SoC has two Asynchronous Communications Interface Adapter (ACIA) modules used to transfer information to and from various communications modules such as LoRa, GSM, Bluetooth, Wi-Fi radio modules and UART enabled devices. See the Memory Map for base addresses. The baud rates are derived from 1.8432MHz XTLI input.

2.8.1 ACIA Register Descriptions

Address = Base + 3		ACIA_CTRL: ACIA Control Register					Reset Value = 0x00	
7:0->	SBN	WL1	WL0	RSC	SBR3	SBR2	SBR1	SBR0
HWRES	0	0	0	1	0	0	0	0
SWRES	-	-	-	1	-	-	-	-

Bit	Name	Access	Description
7	SBN	R/W	1 = 2 Stop bits, 1 ½ Stop bits for WL = 5, 1 Stop bit for WL = 8 and parity
			0 = 1 Stop bit
6	WL1	R/W	11 = 5 bits
			10 = 6 bits
5	WL0	R/W	01 = 7 bits
			00 = 8 bits
4	RSC	R/W	1 = Baud rate
			0 = RSC clock source
3	SBR3	R/W	1110 = 9600, 1111 = 19200
			1100 = 4800, 1101 = 7200
2	SBR2	R/W	1010 = 2400, 1011 = 3600
			1000 = 1200, 1001 = 1800
1	SBR1	R/W	0110 = 300, 0111 = 600
			0100 = 134.58, 0101 = 150
0	SBR0	R/W	0010 = 75, 0011 = 109.92
			0000 = 115.2K, 0001 = 50

Address = Base + 2	ACIA_CMR: ACIA Command Register						Reset Value = 0x00	
7:0->	PCM1	PCM0	PME	REM	TIC1	TIC0	IRD	DTR
HWRES	0	0	0	0	0	0	0	0
SWRES	-	-	-	0	0	0	0	0

Bit	Name	Access	Description
7	PCM1	R/W	11 = Space parity
			10 = Mark parity
6	PCM0	R/W	01 = Odd parity
			00 = Even parity
5	PME	R/W	1 = Parity enabled
			0 = Parity disabled
4	REM	R/W	1 = Receiver Echo Mode not available
			0 = Receiver Echo Mode not available
3	TIC1	R/W	11 = RTSB = low, Transmitter interrupt disabled, Transmit Break
			10 = RTSB = low, Transmitter interrupt disabled
2	TIC0	R/W	01 = RTSB = low, Transmitter interrupt enabled
			00 = RTSB = high, Transmitter interrupt disabled
1	IRD	R/W	1 = Receiver Interrupt Disabled
			0 = Receiver Interrupt Enabled
0	DTR	R/W	1 = Data Terminal Ready
			0 = Data Terminal Transmitter Not Ready

Address = Base + 1		ACIA_STR: ACIA Status Register					Reset Value = 0x10	
7:0->	IRQ	DSRB	DCDB	TDRE	RDRF	OVRN	FE	PE
HWRES	0	0	0	1	0	0	0	0
SWRES	-	-	-	1	-	-	-	-

Bit	Name	Access	Description
7	IRQ	R/O	1 = Interrupt has occurred
			0 = No Interrupt
6	DSRB	R/O	1 = Not ready and not clear to send data
			0 = Ready and clear to send data
5	DCDB	R/O	1 = DCD Not Detected
			0 = DCD Detected
4	TDRE	R/O	1 = Empty
			0 = Not Empty
3	RDRF	R/O	1 = Full
			0 = Not Full
2	OVRN	R/O	1 = Overrun has occurred
			0 = No overrun
1	FE	R/O	1 = Framing error detected
			0 = No framing error
0	PE	R/O	1 = Parity error detected
			0 = No parity error
Address = Base + 1		W/O	Program Reset aka SWRES

Address = Base		ACIA_DR: ACIA Data Register					Reset Value = 0x00	
7:0->	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

Bit	Name	Access	Description
7 - 0	DR[7-0]	R/W	R = Read Receiver Data Register
			W = Write Transmitter Data Register

2.9 I2C Interface Module

For the I2C register descriptions and I2C Operation, refer to the "I2C Design Specification".

2.9.1 I2C Status Register Definitions

Address = Base + 5		SR: I2C Status Register					Reset Value = 0x00	
7:0->	RxACK	WCOL	BUSY	RESERVED	WFFULL	WFEMPTY	RFFULL	RFEMPTY
Bit	**Name**	**Access**	**Description**					
7	RxACK	R/O	1 = No acknowledge received					
			0 = Acknowledge received					
6	BUSY	R/W	1 = After start I2C bus busy signal detected					
			0 = After stop I2C bus busy signal detected					
5	RSRVD	R/O	1 = Never					
			0 = Always					
4	RSRVD	R/O	1 = Never					
			0 = Always					
3	RSRVD	R/O	1 = Never					
			0 = Always					
2	RSRVD	R/O	1 = Never					
			0 = Always					
1	TIP	R/O	1 = Transfer in progress when transferring data					
			0 = When transfer complete					
0	IF	R/O	1 = Interrupt is set when one byte is transferred, processor interrupt request if IEN bit is set.					
			0 = No interrupt					

2.9.2 I2C Command Register Definitions

Address = Base + 4		CR: I2C Command Register					Reset Value = 0x00	
7:0->	STA	STO	RD	WR	ACK	RSVRD	RSVRD	IACK

Bit	Name	Access	Description
7	STA	R/W	1 = Generate start condition
			0 = Do not generate start condition
6	STO	R/W	1 = Generate stop condition
			0 = Do not generate stop condition
5	RD	R/W	1 = Read from slaver
			0 = Do not read from slave
4	WR	R/W	1 = Write slave
			0 = Do not write slave
3	ACK	R/W	1 = NACK
			0 = ACK
2	RSVRD	R/W	1 = Never
			0 = Always
1	RSVRD	R/W	1 = Never
			0 = Always
0	IACK	R/W	1 = Clear a pending interrupt
			0 = Don't clear a pending interrupt

2.9.3 I2C Receive Register Definitions

Last byte received via I2C.

Address = Base + 3		RXR: I2C Receive Register					Reset Value = 0x00	
7:0->	RXR7	RXR6	RXR5	RXR4	RXR3	RXR2	RXR1	RXR0

Bit	Name	Access	Description
7 - 0	RXR[7-0]	R/O	**R = Read Receiver Data Register**
			W = no operation

2.9.4 I2C Transmit Register Definitions

7:1 RW Next byte to transmit via I2C 0 RW In case of a data transfer this bit represent the data's LSB. In case of a slave address transfer this bit represents the RW bit. '1' for reading from slave '0' for writing to slave

Address = Base + 2		TXR: I2C Transmit Register					Reset Value = 0x00	
7:0->	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
Bit	**Name**	**Access**	**Description**					
7 - 0	TXR[7-0]	R/W	R = Read Receiver Data Register					
			W = Write Transmitter Data Register					

2.9.5 I2C Control Register

The core responds to new commands only when the 'EN' bit is set. Pending commands are finished. Clear the 'EN' bit only when no transfer is in progress, i.e. after a STOP command, or when the command register has the STO bit set. When halted during a transfer, the core can hang the I2C bus.

Address = Base +1		CTR: I2C Control Register					Reset Value = 0x10	
7:0->	EN	IEN	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD	RSRVD
Bit	**Name**	**Access**	**Description**					
7	EN	R/W	1 = I2C Core enabled					
			0 = I2C Core disabled					
6	IEN	R/W	1 = I2C Core interrupt enabled					
			0 = I2C Core interrupt disabled					
5	RSRVD	R/W	1 = Never					
			0 = Always					
4	RSRVD	R/W	1 = Never					
			0 = Always					
3	RSRVD	R/W	1 = Never					
			0 = Always					
2	RSRVD	R/W	1 = Never					
			0 = Always					
1	RSRVD	R/W	1 = Never					
			0 = Always					
0	RSRVD	R/W	1 = Never					
			0 = Always					

2.9.6 I2C Clock Prescale Register Definitions

For the I2C register descriptions, refer to the "I2C Design Specification".

This register is used to prescale the SCL clock line. Due to the structure of the I2C interface, the core uses a 4*SCL clock internally. The prescale register must be programmed to this 4*SCL bitrate. Change the value of the prescale register only when the 'EN' bit is cleared.
Example: CLK_I = 32MHz, desired SCL = 100 KHz
Prescale = 32MHZ = 80 (dec) = 50 (hex) 4 * 100 KHz
Reset value: 0xFFFF

Address = Base		PRER: I2C Clock Prescale Register					Reset Value = 0xFF	
7:0->	PRER7	PRER6	PRER5	PRER4	PRER3	PRER2	PRER1	PRER0
Bit	**Name**	**Access**	**Description**					
7 - 0	PRER[7-0]	R/W	R = Read Receiver Data Register					
			W = Write Transmitter Data Register					

2.10 SPI Module

The SPI module described in the standard SPI Specification found in this link.

2.10.1 SPI Extension Register

Address = Base + 3		SPER: SPI Extension Register						Reset Value = 0x00	
7:0->	ICNT1	ICNT0	RESERVED	RESERVED	RESERVED	RESERVED		ESPR1	ESPR0
Bit	**Name**	**Access**	**Description**						
7	ICNT1	R/W	11 = SPIF is set after every four completed transfers						
			10 = SPIF is set after every three completed transfers						
6	ICNT0	R/W	01 = SPIF is set after every two completed transfers						
			00 = SPIF is set after every completed transfer						
5	RESERVED	R/W	1 = Never						
			0 = Always						
4	RESERVED	R/W	1 = Never						
			0 = Always						
3	RESERVED	R/W	1 = Never						
			0 = Always						
2	RESERVED	R/W	1 = Never						
			0 = Always						
1	ESPR1	R/W	11 = Reserved, do not use						
			10 = Add these two bits to the SPI Clock Rate 0=512, 01=1024, 02=2048, 03=4096						
0	ESPR0	R/W	01 = Add these two bits to the SPI Clock Rate 0=8, 01=64, 02=128, 03=256						
			00 = Add these two bits to the SPI Clock Rate 00=2, 01=4, 02=16, 03=32						

2.10.2 SPI Data Register

Address = Base + 2		SPDR: SPI Data Register					Not Initialized on Reset	
7:0->	SPDR7	SPDR6	SPDR5	SPDR4	SPDR3	SPDR2	SPDR1	SPDR0
Bit	**Name**	**Access**	**Description**					
7 - 0	SPDR[7-0]	R/W	R = Read SPI Data buffer					
			W = Write SPI Data buffer					

2.10.3 SPI Status Register

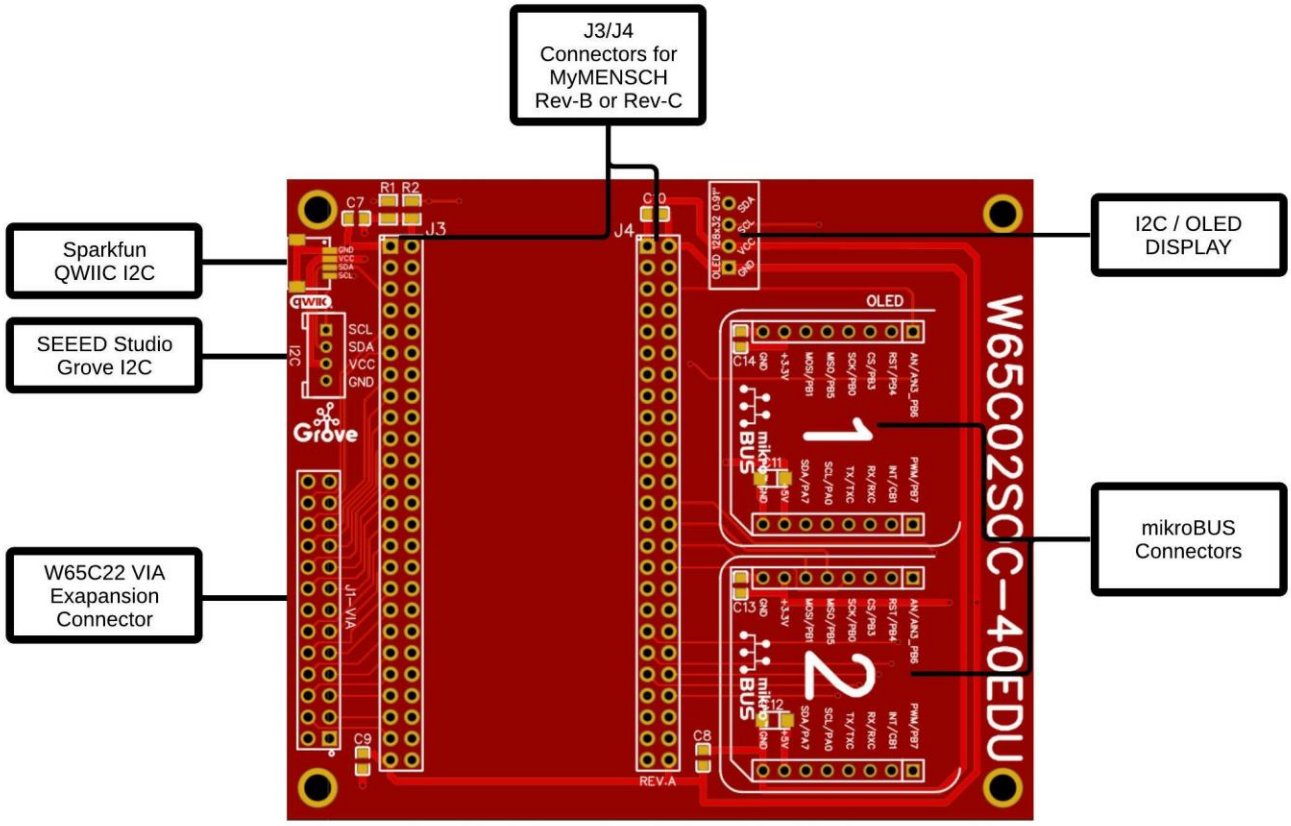
Address = Base + 1		SPSR: SPI Status Register							Reset Value = 0x05
7:0->	SPIF	WCOL	RESERVED	RESERVED	WFFULL	WFEMPTY	RFFULL	RFEMPTY	
Bit	**Name**	**Access**	**Description**						
7	SPIF	R/W	1 = SPI Interrupt Flag is set on completion of a transfer block						
			0 = SPI not interrupting						
6	WCOL	R/W	1 = SPI Core write collision when SPI data register when Write FIFO is full						
			0 = SPI Core disabled						
5	RESERVED	R/O	1 = Never						
			0 = Always						
4	RESERVED	R/O	1 = Never						
			0 = Always						
3	WFFULL	R/O	1 = Write FIFO full						
			0 = Write FIFO not full						
2	WFEMPTY	R/O	1 = Write FIFO empty						
			0 = Write FIFO not empty						
1	RFFULL	R/O	1 = Read FIFO full						
			0 = Read FIFO not full						
0	RFEMPTY	R/O	1 = Read FIFO empty						
			0 = Read FIFO not empty						

2.10.4 SPI Control Register

Address = Base		SPCR: SPI Control Register					Reset Value = 0x10	
7:0->	SPIE	SPE	RESERVED	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	**Name**	**Access**	**Description**					
7	SPIE	R/W	1 = SPI Interrupt Enabled					
			0 = SPI Interrupt Disabled					
6	SPE	R/W	1 = SPI Core enabled					
			0 = SPI Core disabled					
5	RESERVED	R/W						
4	MSTR	R/W	1 = Master					
			0 = Slave					
3	CPOL	R/W	1 = Negative Clock Polarity					
			0 = Positive Clock Polarity					
2	CPHA	R/W	1 = Clock Phase Not Shifted					
			0 = Clock Phase Shifted					
1	SPR1	R/W	These values are used with the ESPR bits to determine the extended clock rate.					
			Refer to the SPI Datasheet for detailed selection information.					
0	SPR0	R/W	These values are used with the ESPR bits to determine the extended clock rate.					
			Refer to the SPI Datasheet for detailed selection information.					

3 W65C02SOC-40EDU Information

3.1 W65C02SOC-40EDU Board Diagram



3.50" x 3.00" PCB

3.2 Left IO Connector J3 on MyMENSCH™

The J3 left connector has 46 IO, 2x 3v3 power and 2x VSS pins. Ball assignments labeled NA are Non-Assigned pins.

J3 – Left Expansion Connector					
Pin	***Signal Name***	***FPGA Ball***	***Pin***	***Signal Name***	***FPGA Ball***
1	VSS	-	2	VDD	-
3	I2C_SCL	L4	4	NA	L3
5	I2C_SDA	K6	6	NA	K5
7	NA	H4	8	NA	N2
9	VIA_A_CB2	M4	10	NA	N3
11	VIA_A_CB1	M5	12	NA	N4
13	VIA_A_PB7	L5	14	NA	N5
15	VIA_A_PB6	N7	16	NA	N6
17	VIA_A_PB5	N8	18	NA	M7
19	VIA_A_PB4	M9	20	NA	M8
21	VIA_A_PB3	M10	22	NA	N9
23	VIA_A_PB2	M11	24	NA	N10
25	VIA_A_PB1	N12	26	NA	N11
27	VIA_A_PB0	M13	28	NA	M12
29	VIA_A_PA7	L13	30	NA	L12
31	VIA_A_PA6	K13	32	NA	K12
33	VIA_A_PA5	K8	34	NA	J8
35	VIA_A_PA4	J9	36	NA	L10
37	VIA_A_PA3	K10	38	NA	L11
39	VIA_A_PA2	K11	40	NA	J10
41	VIA_A_PA1	H9	42	NA	H10
43	VIA_A_PA0	J12	44	NA	J13
45	VIA_A_CA1	H13	46	NA	G12
47	VIA_A_CA2	G13	48	NA	F12
49	VDD	-	50	VSS	-

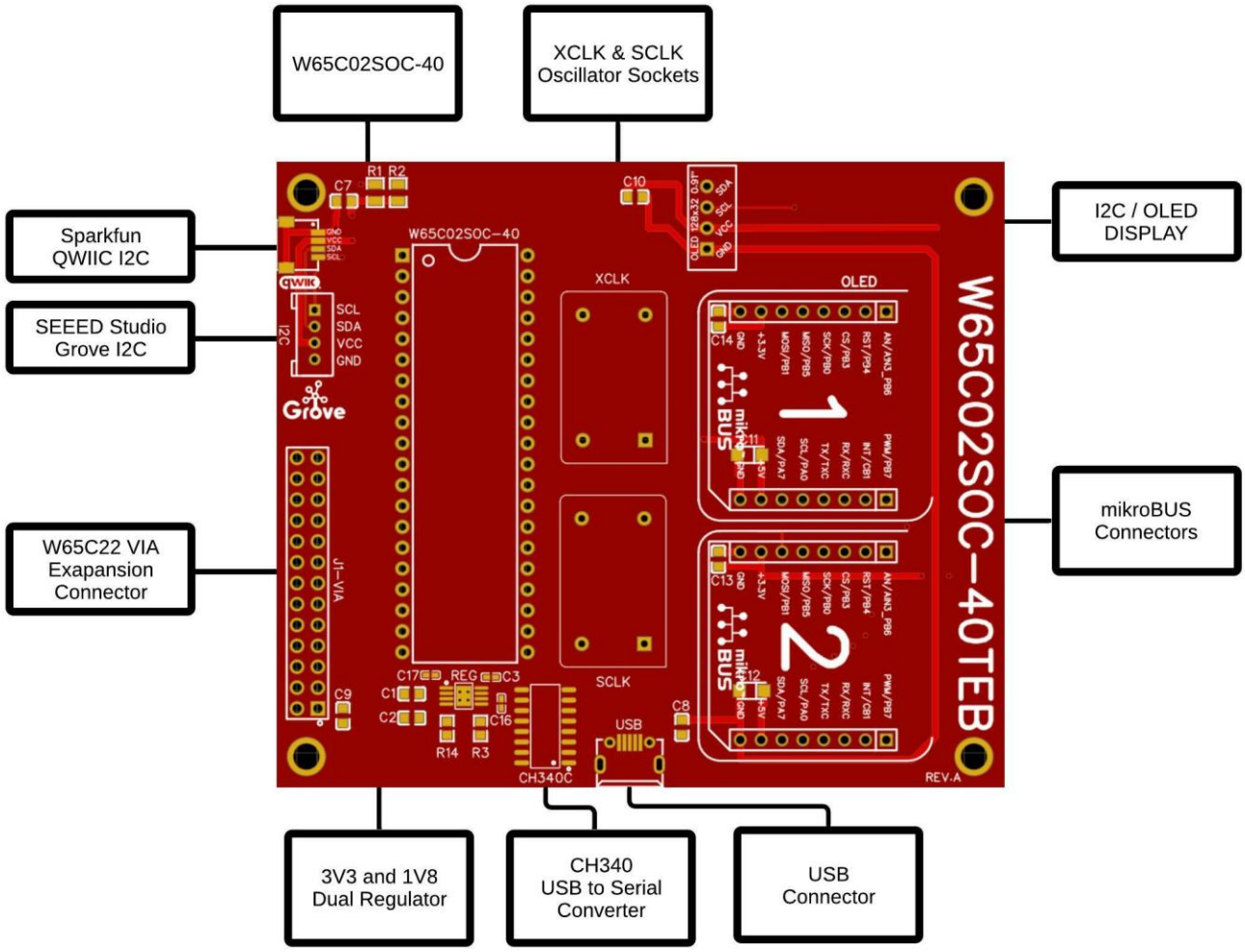
3.3 Right IO Connector J4 on MyMENSCH™

The J4 right connector has 46 IO, 2x 3v3 power and 2x VSS pins. Ball assignments labeled NA are Non-Assigned pins. The ADC inputs are not used for this build and should not be connected to anything.

J4 – Right Expansion Connector					
Pin	***Signal Name***	***FPGA Ball***	***Pin***	***Signal Name***	***FPGA Ball***
1	VDD	-	2	VSS	-
3	NA	H3	4	AGND	(G2)
5	NA	H1	6	ADC_IN0	(F5)
7	NA	H2	8	3v3REF	(F6)
9	DNU/ADC_IN5	F1	10	5vBAT	(G1)
11	DNU/ADC_IN6	E1	12	NA	(E5)
13	DNU/ADC_IN7	C1	14	DNU/ADC_IN1	D1
15	DNU/ADC_IN8	B1	16	DNU/ADC_IN2	C2
17	NA	B2	18	DNU/ADC_IN3	E3
19	NA	A2	20	DNU/ADC_IN4	E4
21	NA	B3	22	XCLK	E6
23	NA	B4	24	SCLK	A3
25	NA	B5	26	SPI_CS0	A4
27	NA	B6	28	SPI_SDI	A5
29	NA	B7	30	SPI_SDO	A6
31	NA	A7	32	SPI_SCLK	D9
33	NA	A8	34	NA	E8
35	NA	C9	36	NA	F8
37	NA	C10	38	NA	A9
39	NA	B10	40	NA	A10
41	NA	B11	42	TXD_B	A11
43	NA	B12	44	RXD_B	A12
45	NA	B13	46	RTSB_B_E6	C11
47	NA	C13	48	CTSB_B_E2	C12
49	VSS	-	50	VDD	-

4 W65C02SOC-40TEB Information

4.0 W65C02SOC-40TEB Board Diagram



3.50" x 3.00" PCB

DIP Socket on W65C02SOC-40TEB

U1 – W65C02SOC-40TEB DIP Socket			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	VSS	40	VSS
2	PA0	39	CA1
3	PA1	38	CA2
4	PA2	37	SPI_SCLK
5	PA3	36	SPI_SDI
6	PA4	35	SPI_SDO
7	PA5	34	SPI_CS0
8	PA6	33	XCLK
9	PA7	32	SCLK
10	PB0	31	TXD_B
11	PB1	30	RXD_B
12	PB2	29	RTSB_B_E6
13	PB3	28	CTSB_B_E2
14	PB4	27	TXD_A
15	PB5	26	RXD_A
16	PB6	25	RTSB_A_E7
17	PB7	24	CTSB_A_E3
18	CB1	23	I2C_SCL
19	CB2	22	I2C_SDA
20	3V3	21	1V8

4.1 USB Code Port on W65C02SOC-40TEB

The Micro USB connector is dual purpose. It is both the power connector that powers the board and the USB code port. The CH340 chip that interfaces to the connector has been pre-programmed so that when the board is power from a USB power on a computer, the chip will request 500mA of current from the host machine. The board can also be powered by any USB port that supplies 5V DC. Note that the board has a 3v3 and 1v8 voltage regulators.

In addition to the power, the USB port serves as an interface to WDC's tool suite for debugging and loading programs into the onboard SRAM.

5 FCC Compliance

The Western Design Center, Inc. (WDC) provides the enclosed product under the following conditions: This board is intended for use for Education, Engineering Development or Evaluation Purposes ONLY and is not considered by WDC to be a finished consumer product. This board should be handled with caution using good electronics handling practices. This board is compliant per RoHS/Green directives. It does not fall within the scope of directives such as FCC, CE, and UL. It generates uses and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules.

6 Ordering Information

The W65C02SOC-40EDU and W65C02SOC-40TEB are available from WDC as part of the W65C02SOC-40 VLSI SOC Design Course.