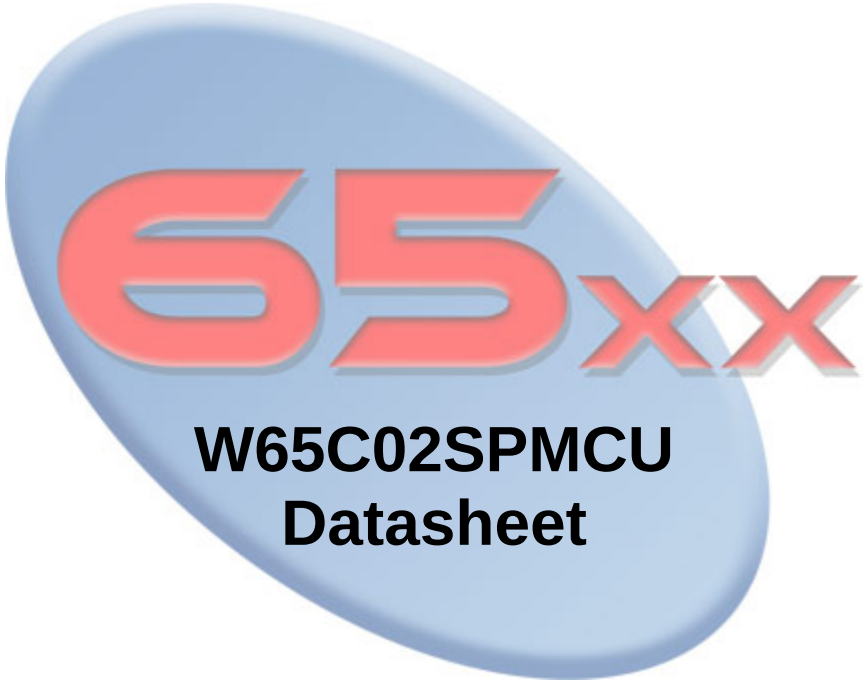

W65C02SPMCU Datasheet

1.1 DOCUMENT REVISION HISTORY

Version	Date	Author	Description
1.0	12/02/09	David Gray	Initial Document Release

1.2 INTRODUCTION

The W65C02SPMCU Terbium Developer Kit (TDK) is a minimal System on Programmable Chip example based on WDC's Verilog IP Cores. This controller uses the W65C02SRTL as the processor and provides the user with a complete kit to begin application development and familiarization with the 65xx technology family. This controller was designed for WDC's Terbi-ECP2Mulator and is part of the Terbium Developer Kit (TDK). This board features a Lattice ECP2M50. A separate user guide is available for the Terbi-ECP2Mulator.

The software platform of the TDK is made up an easy to customize embedded monitor and WDC's ProSDK Tool Suite. The monitor provides in-circuit debug capabilities tethering the features of the hardware and ProSDK. The ProSDK Tool Suite provides all of the application development tools needed including: IDE, Instruction Set Simulator, Debugger, Assemblers, ANSI/ISO Standard Compilers, Optimizers, Linker, Symbol Tool, and Librarian.

KEY FEATURES OF THE W65C02SPMCU

- W65C02SRTL Microprocessor Core
- 32K x 8 FlashROM on chip
- 32K x 8 SRAM on chip
- General Purpose IO modules (2 used for Parallel TIDE Port Interface, 2 for USB TIDE Port Interface, 1 for LEDs Interface, 2 for Dual 7-Segment LED, 1 for User pushbuttons and HEX Input)
- Programmable Hardware Breakpoint for added in-circuit debug
- ProSDK Tool Suite for 65xx Assembly/ANSI/ISO Standard C application development

MEMORY MAP

Start	End	Size	Description
0x8000	0xFFFF	32 KB	32KB Internal ROM
0x7F00	0x7FFF	256 B	256 Byte SRAM Used by WDC Monitor
0x7EFA	0x7EFF	6 B	6 Bytes Shadow Vectors Used by WDC Monitor
0x7E80	0x7EF9	122 B	122 Bytes RAM Reserved for WDC Monitor
0x7E30	0x7E7F	80 B	80 Bytes Reserved for IO
0x7E2C	0x7E2F	4 B	GPIO7 Registers (Pushbuttons and Hex)
0x7E28	0x7E2B	4 B	GPIO6 Registers (LEDs)
0x7E24	0x7E27	4 B	GPIO5 Registers (USB-TIDE CTRL Reg)
0x7E20	0x7E23	4 B	GPIO4 Registers (USB-TIDE Data Reg)
0x7E1C	0x7E1F	4 B	GPIO3 Registers (Left 7-Segment)
0x7E18	0x7E1B	4 B	GPIO2 Registers (Right 7-Segment)
0x7E14	0x7E17	4 B	GPIO1 Registers (Parallel TIDE Port)
0x7E10	0x7E13	4 B	GPIO0 Registers (Parallel TIDE Port)
0x7E00	0x7E0F	16 B	Hardware Breakpoint Registers
0x0200	0x7DFF	31744 B	31744 Byte Internal USER SRAM
0x0100	0x01FF	256 B	Stack Page Memory
0x0000	0x00FF	256 B	Zero Page Memory

2 MODULE DESCRIPTIONS

2.1 W65C02SRTL MODULE

The W65C02S Microprocessor Programming Model, Status Register Coding, and Vector Table, are shown below. Please refer to WDC's W65C02S datasheet for complete information.

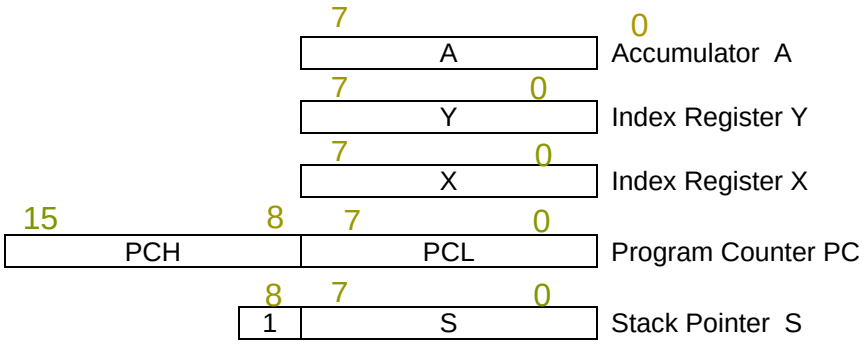

Figure 2.3.1 W65C02S Microprocessor Programming Model

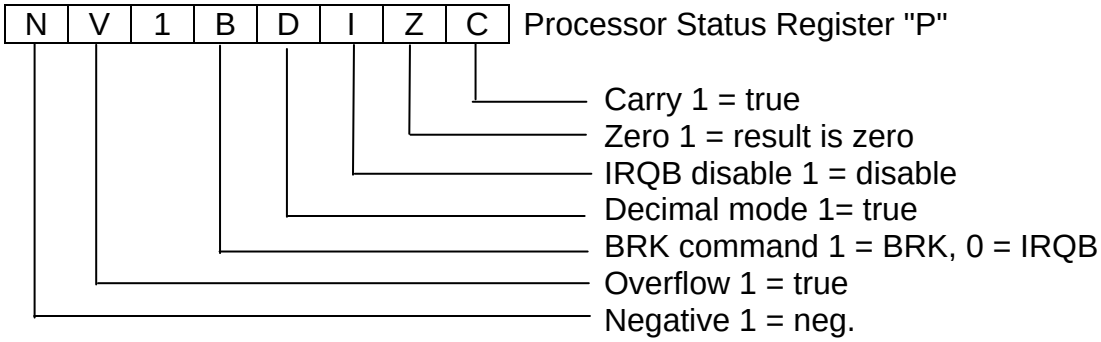

Figure 2.3.2 W65C02S Status Register Coding

Address	Label	Function
FFFF,E	IRQBRK	BRK Vector High, Low
FFFD,C	IRQRES	RES Vector High, Low
FFFB,A	NMI	Non-Maskable Interrupt Vector High, Low

Table 2-5 Vector Table

2.2 GPIO MODULE

The General Purpose Input/Output (GPIO) Module is used to transfer information to and from the board using either WDC's embedded Terbium IDE (TIDE) monitor or custom IO software for control, test or debug purposes.

The Handshake Input (HSI) pin is used to handshake data into the GPIO port through the bi-directional 8 data pins. The Handshake Output (HSO) pin is used to handshake data output on the GPIO port data pins.

The 8 IO data pins can be set individually as inputs or outputs with the Data Direction Register (DDR) of the GPIO Module.

2.2.1 GPIO Module Register Descriptions

Address = 0x7E(1/2)3/7/B/F		GPIO_CTRL_STAT: GPIO Control/Status Register					Reset Value = 0x02	
7:0->	GIRQ	HIL	HIE	TEST	0	0	HLOM	HIES

Bit	Name	Access	Description
7	GIRQ	R/O	1 = GPIO Interrupt Occurred (selected edge on HSI input)
			0 = No GPIO Interrupt Occurred
6	HIL	R/O	1 = HSI Input Level high (DSR not ready)
			0 = HSI Input Level low (DSR ready)
5	HIE	R/W	1 = HSI Interrupt enabled (GIRQ Interrupt enabled)
			0 = HSI Interrupt not enabled
4	TEST	R/W	1 = Test with HSI connected to HSO
			0 = Normal mode
1	HLOM	R/W	1 = HSO Level Output mode Set to high
			0 = HSO Level Output mode to low (active)
0	HIES	R/W	1 = HSI Interrupt Edge select set to Positive edge
			1 = HSI Interrupt Edge select set to Negative edge

Address = 0x7E(1/2)2/6/A/E		GPIO_DDR: GPIO Data Direction Register					Reset Value = 0x00	
7:0->	DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0

Bit	Name	Access	Description
7 - 0	DDR[7:0]	R/W	1 = PIO data direction set to Output (bit 7 for PIO7, bit 0 for PIO0)
			0 = PIO data direction set to Input (bit 7 for PIO7, bit 0 for PIO0)

Address = 0x7E(1/2)1/5/9/D		GPIO_PUER: GPIO Pull-Up Enable Register					Reset Value = 0xFF	
7:0->	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0

Bit	Name	Access	Description
7 - 0	PUE[7:0]	R/W	1 = Pull-up on PIO Enabled (bit 7 for PIO7, bit 0 for PIO0)
			0 = Pull-up on PIO Disabled (bit 7 for PIO7, bit 0 for PIO0)

Address = 0x7E(1/2)0/4/8/C		GPIO_DATA: GPIO Data Register					Reset Value = 0x00	
7:0->	PIO7	PIO6	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0
Bit	**Name**	**Access**	**Description**					
7 - 0	PIO[7:0]	R/W	1 = PIO line is logic 1 (returns value of PIO line on read, sets value to assert PIO on write)					
			0 = PIO line is logic 0 (returns value of PIO line on read, sets value to assert PIO on write)					

2.3 Hardware Breakpoint Module (HBM) Module

A Hardware Breakpoint Match pulls NMIB low. Address 0F is the Control Register. The monitor needs to write a “0” into the Control Register after a breakpoint has been read to clear it. Writing a “1” to Bit 7 will cause a manual NMI if the breakpoint is enabled.

Address	RTL Label	Description
0	BRKREG0	Address byte 0 (bits 0-7)
1	BRKREG1	Address byte 1 (bits 8-15)
2	BRKREG2	Address byte 2 (bits 16-23)
3	BRKREG3	Address byte 3 (bits 24-31) Reserved
4	DATREG0	Data Compare Value byte 0 (bits 0-7)
5	DATREG1	Data Compare Value byte 1 (bits 8-15) Reserved
6	DATREG2	Data Compare Value byte 2 (bits 16-23) Reserved
7	DATREG3	Data Compare Value byte 3 (bits 24-31) Reserved
8	Reserved	
9	Reserved	
A	Reserved	
B	Reserved	
C	Reserved	
D	Reserved	
E	Reserved	
F	ICDCTRL	ICD Control Register

2.3.1 Hardware Breakpoint Module (HBM) Register Descriptions

Address = 0x7E0F		HBM_ICDCTRL: Hardware Breakpoint Control					Reset Value = 0x00	
7:0->	BRK	0	0	0	MATCH	DATAEN	RWSEL	BRKEN
Bit	**Name**	**Access**	**Description**					
7	BRK	R/W	1 = Hardware Break occurred					
			0 = No Hardware Break occurred					
3	MATCH	R/W	1 = Data breakpoint if DATAREG value matches bus value					
			0 = Data breakpoint if DATAREG value doesn't match bus value					
2	DATAEN	R/W	1 = Enable breakpoint on data bus and DATAREG match (or mismatch as selected by bit 3)					
			0 = Disable breakpoint on Data					
1	RWSEL	R/W	1 = Data breakpoint on Read data (in to MPU)					
			0 = Data breakpoint on Write data (out from MPU)					
0	BRKEN	R/W	1 = Enable breakpoint on match with Address in BRKREG register					
			0 = Disable Address breakpoint					

Address = 0x7E04		HBM_DATAREG: Hardware Data Match					Reset Value = 0x00	
7:0->	DVAL7	DVAL6	DVAL5	DVAL4	DVAL3	DVAL2	DVAL1	DVAL0
Bit	**Name**	**Access**	**Description**					
7 - 0	DVAL[7:0]	R/W	Value of Data bus to match or mismatch with (as selected by ICDCTRL register)					
			bits 7-0 correspond to MPU data bus signals 7-0 for matching or not-matching					

Address = 0x7E01		HBM_BRKREG_H: Hardware Breakpoint Address (High Byte)					Reset Value = 0x00	
7:0->	BADR15	BADR14	BADR13	BADR12	BADR11	BADR10	BADR9	BADR8
Bit	**Name**	**Access**	**Description**					
7 - 0	BADR[15:8]	R/W	Value of Address bus to match with					
			bits 15-0 correspond to MPU address bus signals 15-0 for matching					

Address = 0x7E00		HBM_BRKREG_L: Hardware Breakpoint Address (Low Byte)					Reset Value = 0x00	
7:0->	BADR7	BADR6	BADR5	BADR4	BADR3	BADR2	BADR1	BADR0
Bit	**Name**	**Access**	**Description**					
7 - 0	BADR[7:0]	R/W	Value of Address bus to match with					
			bits 15-0 correspond to MPU address bus signals 15-0 for matching					

2.4 USBGPIO Interface for USB TIDE Port

USB interface for use with TIDE and WDC-DB PC software on the Terbi board. This module interfaces with the FTDI 245R chip. This interface uses 2 GPIO modules. The GPIO Data Register is described below for both GPIO Ports.

2.4.1 USBGPIO Module Register Descriptions

0x7E24		GPIO5 Data - TIDE USB Status and Control Register	
Bit	**Access**	**Bit Name**	**Description**
7	R/O	TxEmpty_B	If set, then data register can be written to
6	R/O	RxFull_B	If set low, then data register contains valid data to be read
5	R/W	ReadStrobe_B	Read pulse out to the USBFIFO
4	R/O	Reset_B	If set, then normal mode, if clear, then ESC-ESC rx'ed
3	R/O	PowerEnable_B	If set, then FTDI chip finished USB enumeration
2-0	-	-	Not Used

Address = 0x7E(1/2)3/7/B/F		GPIO_CTRL_STAT: GPIO Control/Status Register					Reset Value = 0x02	
7:0->	**GIRQ**	**HIL**	**HIE**	**TEST**	**0**	**0**	**HLOM**	**HIES**
Bit	**Name**	**Access**	**Description**					
7	GIRQ	R/O	1 = GPIO Interrupt Occurred (selected edge on HSI input)					
			0 = No GPIO Interrupt Occurred					
6	HIL	R/O	1 = HSI Input Level high (DSR not ready)					
			0 = HSI Input Level low (DSR ready)					
5	HIE	R/W	1 = HSI Interrupt enabled (GIRQ Interrupt enabled)					
			0 = HSI Interrupt not enabled					
4	TEST	R/W	1 = Test with HSI connected to HSO					
			0 = Normal mode					
1	HLOM	R/W	1 = HSO Level Output mode Set to high					
			0 = HSO Level Output mode to low (active)					
0	HIES	R/W	1 = HSI Interrupt Edge select set to Positive edge					
			1 = HSI Interrupt Edge select set to Negative edge					

Address = 0x7E20		GPIO_DATA: TIDE USB Data Register					Reset Value = 0x00	
7:0->	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Bit	**Name**	**Access**	**Description**					
7 - 0	DATA	R/W	RX (read) and TX (write) Data					