YESTERDAY, TODAY, AND TOMORROW

W65C265S
8/16-bit Microcontroller

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DOCUMENT REVISION HISTORY

Version	Date	Authors	Description
2.0	10/15/2019	Bill Mensch	Rewrite of the W65C265S Datasheet
2.1	05/07/2020	David Gray	Update Pin Description for QFP. Clarification for PLCC package EOL.
2.2	03/18/2024	David Gray	Updated headers and footers.

1 INTRODUCTION

The W65C265S 8/16-bit CMOS Microcontroller is fully static with key features listed below.

This product description assumes that the reader is familiar with the W65C816S 8/16-bit Microprocessor. Refer to the W65C816S 8/16-bit Microprocessor Datasheet for additional information.

1.1 KEY FEATURES OF THE W65C265S

- CMOS process
- Operating TA =0°C to +70°C
- Single 2.8V to 5.5V power supply
- Static to 8MHz clock operation
- W65C816S compatible CPU
    - 8- and 16-bit parallel processing
    - Variable length stack
    - True indexing capability
    - Twenty-four address modes
    - Decimal or binary arithmetic
    - Pipeline architecture
    - Fully static CPU
- Single chip microcomputer
    - 2 Tone Generators
    - 64 CMOS compatible I/O lines
    - 8,192 x 8 ROM on-chip
    - 576 x 8 SRAM on-chip
    - WAIt for interrupt
    - SToP the clock
    - Fast oscillator start and stop feature
- 16Mbyte linear address space
- Twenty-nine priority encoded interrupts
    - BRK software interrupt
    - RESET "RESTART" interrupt
    - NMIB Non-Maskable interrupt
    - ABORT interrupt
    - COP software interrupt
    - IRQB level interrupt
    - 8 timer edge interrupts
    - 6 edge interrupts
    - PIB interrupt
    - 4 UART Receiver interrupts
    - 4 UART Transmitter interrupts
- Four UARTS's
- Time of Day (ToD) clock features
- 8 x 16 bit timer/counters
- Bus Control Register
- Many bus operating features and modes
- 8 Programmable chip select outputs
- Low cost surface mount 84 and 100 lead packages
- Macro and Cross assemblers available
- C compilers available

1.2 Functional Block Diagram
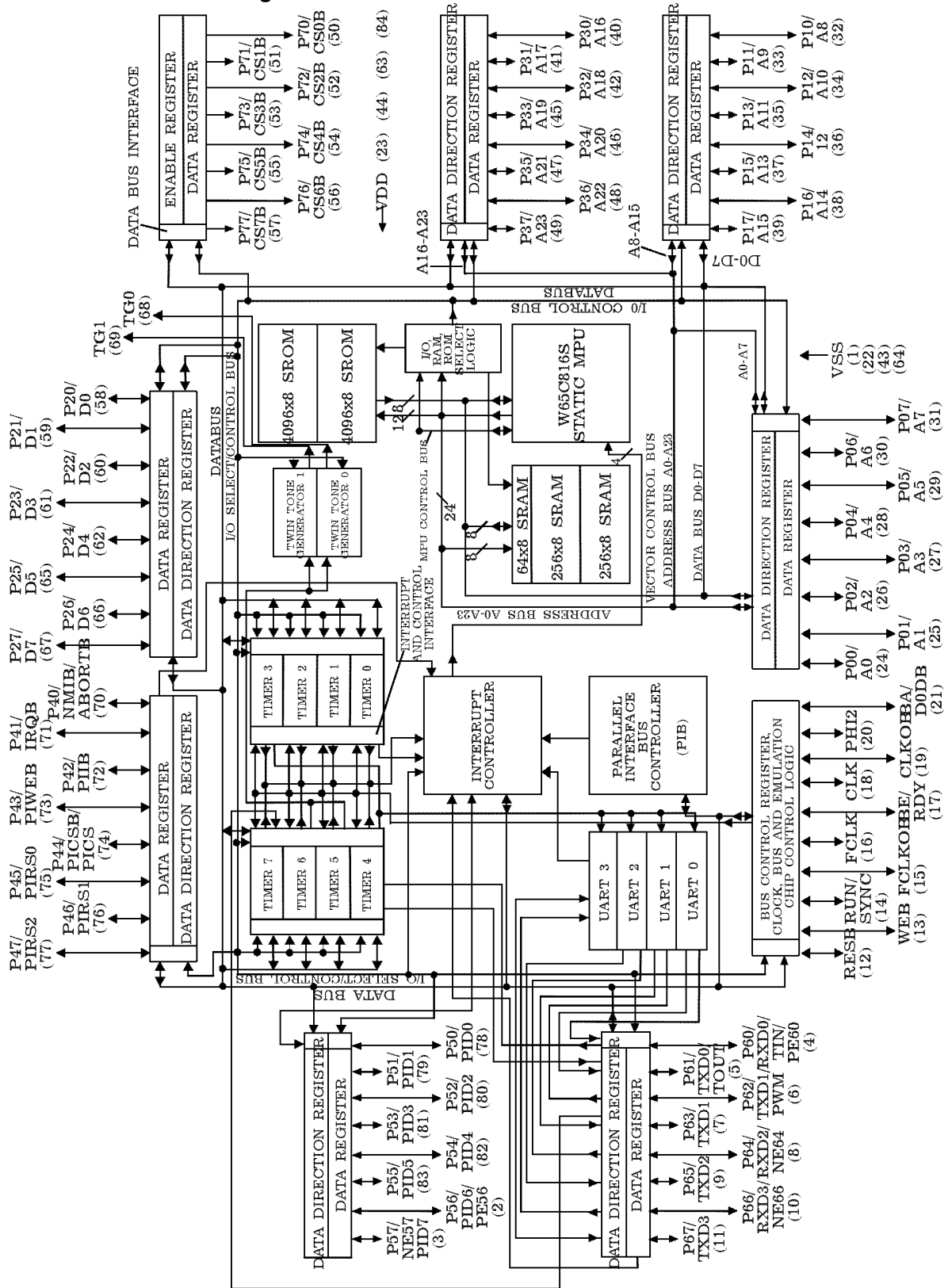
2 FUNCTION DESCRIPTION

2.1 W65C816 Static 8/16-bit Microprocessor Core

The W65C816S 8/16-bit microprocessor is the fully static. The W65C265S has the full 24-bit address and data bus available as opposed to the W65C816S having the high order 16-23 address pin multiplexed with the data bus. The W65C265S is found on the W65C265SXB for easy getting started with the W65C265S IC.

Refer to the W65C816S Microprocessor Datasheet for the Microprocessor Programming Model, Status Register Coding and complete information. More information is found in ***Programming the 65816: Including the 6502, 65C02 and 65802*** Manual available through Amazon.

2.2 Monitor ROM

The W65C265S 8K x 8 bit Read Only Memory (ROM) contains the Mensch Monitor. See the W65C265S Monitor ROM Reference Manual for more information.

2.3 SRAM

The 512 bytes of SRAM are located at 0x0000-0x01FF, and 64 bytes at 0xDF80-0xDFBF for a total of 576 bytes.

2.4 Priority Interrupt Controller Module Information

The Interrupt Control Module controls the priority encoded vectored memory map for interrupts. Each interrupt is connected to the Interrupt Control Module for prioritizing.

Interrupt Enable Registers for the various interrupts are the interrupt enable by the various enable bits. Reading the various IER and IFR bits determines the interrupt that occurred. By prioritizing the interrupts one can determine which interrupt occurred in the associated interrupt handler routine. Notice that any of the 8 interrupts for a GPIO 8-bit port will cause a GPIO vectored interrupt to occur.

2.4.1 Emulation Mode Priority Encoded Interrupt Vector Module

Address	Label	Function
0xFFFE,F	IRQBRK	BRK - Software Interrupt
0xFFFC,D	IRQRES	RES - "REStart" Interrupt
0xFFFA,B	IRQNMI	Non-Maskable Interrupt
0xFFF8,9	IABORT	ABORT Interrupt
0xFFF6,7	IRQRVD	Reserved
0xFFF4,5	IRQCOP	COP Software Interrupt
0xFFF2,3	IRQRVD	Reserved
0xFFF0,1	IRQRVD	Reserved
0xFFEE,F	IRQAT3	UART3 Transmitter Interrupt
0xFFEC,D	IRQAR3	UART3 Receiver Interrupt
0xFFEA,B	IRQAT2	UART2 Transmitter Interrupt
0xFFE8,9	IRQAR2	UART2 Receiver Interrupt
0xFFE6,7	IRQAT1	UART1 Transmitter Interrupt
0xFFE4,5	IRQAR1	UART1 Receiver Interrupt
0xFFE2,3	IRQAT0	UART0 Transmitter Interrupt
0xFFE0,1	IRQAR0	UART0 Receiver Interrupt
0xFFDE,F	IRQ	IRQ Level Interrupt
0xFFDC,D	IRQPIB	Parallel Interface Bus (PIB) Interrupt
0xFFDA,B	IRNE66	Negative Edge Interrupt on P66
0xFFD8,9	IRNE64	Negative Edge Interrupt on P64
0xFFD6,7	IRPE62	Positive Edge Interrupt on P62 for PWM
0xFFD4,5	IRPE60	Positive Edge Interrupt on P60
0xFFD2,3	IRNE57	Negative Edge Interrupt on P57
0xFFD0,1	IRPE56	Positive Edge Interrupt on P56
0xFFCE,F	IRQT7	Timer 7 Interrupt
0xFFCC,D	IRQT6	Timer 6 Interrupt
0xFFCA,B	IRQT5	Timer 5 Interrupt
0xFFC8,9	IRQT4	Timer 4 Interrupt
0xFFC6,7	IRQT3	Timer 3 Interrupt
0xFFC4,5	IRQT2	Timer 2 Interrupt
0xFFC2,3	IRQT1	Timer 1 Interrupt
0xFFC0,1	IRQT0	Timer 0 Interrupt

2.4.2 Native Mode Priority Encoded Interrupt Vector Module

Address	Label	Function
0xFFBE,F	IRQRVD	Reserved
0xFFBC,D	IRQRVD	Reserved
0xFFBA,B	IRQNMI	Non-Maskable Interrupt
0xFFB8,9	IABORT	ABORT Interrupt
0xFFB6,7	IRQBRK	BRK Software Interrupt
0xFFB4,5	IRQCOP	COP Software Interrupt
0xFFB2,3	IRQRVD	COP Software Interrupt
0xFFB0,1	IRQRVD	Reserved
0xFFAE,F	IRQAT3	UART3 Transmitter Interrupt
0xFFAC,D	IRQAR3	UART3 Receiver Interrupt
0xFFAA,B	IRQAT2	UART2 Transmitter Interrupt
0xFFA8,9	IRQAR2	UART2 Receiver Interrupt
0xFFA6,7	IRQAT1	UART1 Transmitter Interrupt
0xFFA4,5	IRQAR1	UART1 Receiver Interrupt
0xFFA2,3	IRQAT0	UART0 Transmitter Interrupt
0xFFA0,1	IRQAR0	UART0 Receiver Interrupt
0xFF9E,F	IRQ	IRQ Level Interrupt
0xFF9C,D	IRQPIB	Parallel Interface Bus (PIB) Interrupt
0xFF9A,B	IRNE66	Negative Edge Interrupt on P66
0xFF98,9	IRNE64	Negative Edge Interrupt on P64
0xFF96,7	IRPE62	Positive Edge Interrupt on P62 for
0xFF94,5	IRPE60	Positive Edge Interrupt on P60
0xFF92,3	IRNE57	Negative Edge Interrupt on P57
0xFF90,1	IRPE56	Positive Edge Interrupt on P56
0xFF8E,F	IRQT7	Timer 7 Interrupt
0xFF8C,D	IRQT6	Timer 6 Interrupt
0xFF8A,B	IRQT5	Timer 5 Interrupt
0xFF88,9	IRQT4	Timer 4 Interrupt
0xFF86,7	IRQT3	Timer 3 Interrupt
0xFF84,5	IRQT2	Timer 2 Interrupt
0xFF82,3	IRQT1	Timer 1 Interrupt
0xFF80,1	IRQT0	Timer 0 Interrupt

2.5 Memory Map

Start	End	Size	Description
C00000	FFFFFF	4MB	CS7B Chip Select 7 for User 4MB Memory
400000	BFFFFF	8MB	CS6B Chip Select for User 8MB Memory
000000	3FFFFF	4MB	CS5B Chip Select for User 4MB-selected Memory (Note 1, 2)
0xE000	0xFFFF	8,192 B	CS4B Monitor ROM (Note 1, 2)
0xDFC0	0xDFFF	64 B	CS1B PIB SRAM Expansion (Note 2)
0xDF80	0xDFBF	64 B	On-Chip PIB SRAM
0xDF70	0xDF7F	16 B	On Chip UART Registers
0xDF50	0xDF6F	32 B	On-Chip Timer Registers
0xDF40	0xDF4F	16 B	On-Chip Control Registers
0xDF20	0xDF27	8 B	On-Chip IO Registers
0xDF00	0xDF1F	32 B	CS0B Port Replacement and Expansion (Note 2, 4)
0xDF00	0xDF07	8 B	On-Chip IO Registers
0x8000	0xDEFF	24,320 B	CS4B External FLASH Program and Data Memory
0x0200	0x7FFF	32,256 B	CS3B External SRAM (Note 2, 3)
0x0000	0x01FF	512 B	On-Chip SRAM

Note 1: When on-chip 8K bytes of ROM are enabled, addresses 0xE000-0xFFFF will not appear in CS4B chip select decode. On Chip addresses 0xDF00-0xDFFF never appear in CS4B or CS5B chip select decode.

Note 2: When on-chip ROM, CS3B and/or CS4B are enabled, then CS5B decode is reduced by the addresses used by same. CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3: When SSCR2 is "0" (internal RAM), then CS3B is active for addresses 0x0200-0x7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses 0x0000-0x7FFF.

Note 4: CS0B is inactive when 0xDF00-0xDF07 are used for internal I/O register select (BCR0=0) when (BCR0=1) external memory bus is enabled CS0B is active for addresses 0xDF00-0xDF1F.

Note 5: CS2B is active indicating whenever on chip SRAM memory or registers are accessed.

2.5.1 Communication Register Memory Map

Address	Label	Function	Reset Value
0xDFC0-FF	RAM	CS1B PIB SRAM Expansion	External
0xDF80-BF	RAM	RAM Registers	uninitialized
0xDF7F	PIR7	Parallel Interface Register 7	uninitialized
0xDF7E	PIR6	Parallel Interface Register 6	uninitialized
0xDF7D	PIR5	Parallel Interface Register 5	uninitialized
0xDF7C	PIR4	Parallel Interface Register 4	uninitialized
0xDF7B	PIR3	Parallel Interface Register 3	uninitialized
0xDF7A	PIR2	Parallel Interface Register 2	uninitialized
0xDF79	PIBER	Parallel Interface Enable Register	$00
0xDF78	PIBFR	Parallel Interface Flag Register	$00
0xDF77	ARTD3	UART 3 Data Register	uninitialized
0xDF76	ACSR3	UART 3 Control/Status Register	$00
0xDF75	ARTD2	UART 2 Data Register	uninitialized
0xDF74	ACSR2	UART 2 Control/Status Register	$00
0xDF73	ARTD1	UART 1 Data Register	uninitialized
0xDF72	ACSR1	UART 1 Control/Status Register	$00
0xDF71	ARTD0	UART 0 Data Register	uninitialized
0xDF70	ACSRO	UART 0 Control/Status Register	$00

2.5.2 Timer Register Memory Map

Address	Label	Function	Reset Value
0xDF6F	T7CH	Timer 7 Counter High	uninitialized
0xDF6E	T7CL	Timer 7 Counter Low	uninitialized
0xDF6D	T6CH	Timer 6 Counter High	uninitialized
0xDF6C	T6CL	Timer 6 Counter Low	uninitialized
0xDF6B	T5CH	Timer 5 Counter High	uninitialized
0xDF6A	T5CL	Timer 5 Counter Low	uninitialized
0xDF69	T4CH	Timer 4 Counter High	uninitialized
0xDF68	T4CL	Timer 4 Counter Low	uninitialized
0xDF67	T3CH	Timer 3 Counter High	uninitialized
0xDF66	T3CL	Timer 3 Counter Low	uninitialized
0xDF65	T2CH	Timer 2 Counter High	uninitialized
0xDF64	T2CL	Timer 2 Counter Low	uninitialized
0xDF63	T1CH	Timer 1 Counter High	uninitialized
0xDF62	T1CL	Timer 1 Counter Low	uninitialized
0xDF61	T0CH	Timer 0 Counter High	uninitialized
0xDF60	T0CL	Timer 0 Counter Low	uninitialized
0xDF5F	T7LH	Timer 7 Latch High	uninitialized
0xDF5E	T7LL	Timer 7 Latch Low	uninitialized
0xDF5D	T6LH	Timer 6 Latch High	uninitialized
0xDF5C	T6LL	Timer 6 Latch Low	uninitialized
0xDF5B	T5LH	Timer 5 Latch High	uninitialized
0xDF5A	T5LL	Timer 5 Latch Low	uninitialized
0xDF59	T4LH	Timer 4 Latch High	uninitialized
0xDF58	T4LL	Timer 4 Latch Low	uninitialized
0xDF57	T3LH	Timer 3 Latch High	uninitialized
0xDF56	T3LL	Timer 3 Latch Low	uninitialized
0xDF55	T2LH	Timer 2 Latch High	uninitialized
0xDF54	T2LL	Timer 2 Latch Low	uninitialized
0xDF53	T1LH	Timer 1 Latch High	uninitialized
0xDF52	T1LL	Timer 1 Latch Low	uninitialized
0xDF51	T0LH	Timer 0 Latch High	uninitialized
0xDF50	T0LL	Timer 0 Latch Low	uninitialized

2.5.3 Control and Status Register Memory Map

Address	Label	Function	Reset Value
0xDF4A-4F	---	Reserved	uninitialized
0xDF49	UIER	UART Interrupt Enable Register	$00
0xDF48	UIFR	UART Interrupt Flag Register	$00
0xDF47	EIER	Edge Interrupt Enable Register	$00
0xDF46	TIER	Timer Interrupt Enable Register	$00
0xDF45	EIFR	Edge Interrupt Flag Register	$00
0xDF44	TIFR	Timer Interrupt Flag Register	$00
0xDF43	TER	Timer Enable Register	$00
0xDF42	TCR	Timer Control Register	$00
0xDF41	SSCR	System Speed Control Register	$00
0xDF40	BCR	Bus Control Register	$00/$89

2.5.4 I/O Register Memory Map

Address	Label	Function	Reset Value
0xDF28-3F	---	Reserved	uninitialized
0xDF27	PCS7	Port 7 Chip Select	$00
0xDF26	PDD6	Port 6 Data Direction Register	$00
0xDF25	PDD5	Post 5 Data Direction Register	$00
0xDF24	PDD4	Port 4 Data Direction Register	$00
0xDF23	PD7	Port 7 Data Register	$FF
0xDF22	PD6	Port 6 Data Register	$00
0xDF21	PD5	Port 5 Data Register	$00
0xDF20	PD4	Port 4 Data Register	$00
0xDF00-1F	CS0	Port Replacement & Expansion	uninitialized
0xDF07	PDD3	Port 3 Data Direction Register	$00
0xDF06	PDD2	Port 2 Data Direction Register	$00
0xDF05	PDD1	Port 1 Data Direction Register	$00
0xDF04	PDD0	Port 0 Data Direction Register	$00
0xDF03	PD3	Port 3 Data Register	$00
0xDF02	PD2	Port 2 Data Register	$00
0xDF01	PD1	Port 1 Data Register	$00
0xDF00	PD0	Port 0 Data Register	$00

2.6 Bus Control Register (BCR)

The Bus Control Register (BCR) controls the various modes of I/O and external memory interface during power-up. The value of BE defines the initial values of BCR0, BCR3 and BCR7, three bits in the BCR that set up the W65C265S for In-Circuit-Emulation (ICE) or normal mode. When BE goes high after RESB goes high the BCR sets up the W65C265S for emulation. Port 0 and 1 are the address outputs, Port 2 is the data I/O bus and RUN is the multiplexed RUN function. (See RUN pin function description).
When the rising edge of BE occurs before the rising edge of RESB, all bits in the BCR are "0". After RESB goes high BE no longer effects the BCR register, and BCR may be written under software control to reconfigure the W65C265S as desired. Table 1-1 and Figure 1-1 (following page) indicate how BCR7 and BE define the W65C265S configuration.

Table 1-1 BCR7 and BE Control

BCR7	BE	W65C265S configuration
0	0	Internal ROM External Processor (DMA test mode)
0	1	Internal ROM Internal Processor
1	0	External ROM External Processor (DMA test mode)
1	1	External ROM Internal Processor

2.6.1 Bus Control Register (BCR) Description

Address = 0xDF40		BCR Register						Reset Value = 0x00	
7:0->	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
HWRES	0 = BE High	0	0	0	0	0	0	0
BERES	1 = BE Low	-	-	-	1	-	-	1
Bit	**Name**	**Access**	**Description**						
7	**BCR7**	R/W	1 = External ROM (BE controls shown in Table 1-1)						
			0 = Internal ROM (BE Controls shown in Table 1-1)						
6	**BCR6**	R/W	1 = Enable NMIB on P40 Input is level sensitive, NMIB and ABORTB cannot both be enabled at the same time.						
			0 = Disable NMIB						
5	**BCR5**	R/W	1 = Enable ABORTB on P40 Input is level sensitive, NMIB and ABORTB cannot both be enabled at the same time.						
			0 = Disable ABORTB						
4	**BCR4**	R/W	1 = Watch Dog Enabled						
			0 = Watch Dog Disabled						
3	**BCR3**	R/W	1 = Emulation Mode, RUN=Run, BA=BA/1 All on-chip addressed memory or I/O for reads or writes are output on the data bus (this is the emulation mode of operation)						
			0 = Normal Operation RUN=RUN, BA=BA						
2	**BCR2**	R/W	1 = Enable TG1						
			0 = Disable TG1						
1	**BCR1**	R/W	1 = Enable TG0						
			0 = Disable TG0						
0	**BCR0**	R/W	1 = Ports 0,1,2,3 are address and data bus pins						
			0 = Ports 0,1,2,3 are I/O pins						

2.7 Timers

Upon Timer clock input negative edge the timer counter is decremented by 1.

A write to the timer low counter writes the timer low latch.

A read of the timer high or low counter reads the timer high or low counter.

Upon Timer clock input negative edge when the timer low counter reaches zero, the timer high counter is decremented by 1. Upon Timer clock input positive edge, when the timer high counter reaches zero, this sequence occurs:

The Timer sets its associated interrupt flag. If the interrupt is enabled the MPU is then interrupted and control is transferred to the vector associated with the interrupt. When the Watch Dog Timer 0 times out, the W65C265S is restarted: on-chip logic pulls RESB pin low for 2 CLK cycles and releases RESB to go high, "restarting" the W65C265S.

The Timer high counter is loaded from the timer high latch, and timer low counter is loaded from timer low latch.

A write to the Timer high counter writes to the timer high latch and this sequence occurs:

The timer high latch is loaded from data bus.

The timer low counter is loaded from the timer low latch, and the timer high counter is loaded from the timer high latch.

The Watch Dog Timer 0 is disabled after RESB and is activated by the first TER0 transition from "0" to "1" resulting in the first load of Timer 0 after the W65C265S has been restarted.

The Timer 0 counter is reloaded with the value in the Timer 0 latches when the TER0 bit 0 makes a transition from a "0" to "1". TER0 transition from a "1" to a "0" has no effect on the timer.
A timer must be reloaded after it is disabled with TERx for it could have been stopped with all $FFFF's and when restarted will require full length count down.

2.7.1 Timer Functions

Number	Timer Function	TCR0=0	TCR0=1
T7	Pulse Width Measurement	FCLK	-
T6	Tone Generator	FCLK	-
T5	Tone Generator	FCLK	-
T4	UART Baud Rate or Pulse, Input/Output	FCLK	P60
T3	UART Baud Rate	FCLK	-
T2	Prescaled Interrupt	FCLK/16	-
T1	Time of Day	CLK	-
T0	Monitor Watch Dog	CLK	-

2.7.2 Timer Control Register (TCR) Description

Address = 0xDF42	TCR: Timer Control Register						Reset Value = 0x00	
7:0->	TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0
Bit	Name	Access	Description					
7	TCR7	R/W	1 = UART3 Timer 4 Selected					
			0 = UART3 Timer 3 Selected					
6	TCR6	R/W	1 = UART2 Timer 4 Selected					
			0 = UART2 Timer 3 Selected					
5	TCR5	R/W	1 = UART1 Timer 4 Selected					
			0 = UART1 Timer 3 Selected					
4	TCR4	R/W	1 = UART0 Timer 4 Selected					
			0 = UART0 Timer 3 Selected					
3	TCR3	R/W	11 = Pulse Width Measurement on P62 Both Edges					
			10 = Pulse Width Measurement on P62 Negative Edges					
2	TCR2	R/W	01 = Pulse Width Measurement on P62 Positive Edges					
			00 = Disable					
1	TCR1	R/W	1 = Enable Timer 4 on P61					
			0 = Disable Timer 4 on P61					
0	TCR0	R/W	1 = Timer 4 Clock Selected on P60					
			0 = Timer 4 FCLK Selected					

2.7.3 Timer Enable Register (TER) Description

Address = 0xDF43		TER: Timer Enable Register					Reset Value = 0x00	
7:0->	TER7	TER6	TER5	TER4	TER3	TER2	TER1	TER0
Bit	Name	Access	Description					
7	TER7	R/W	1 = Timer 7 Enabled					
			0 = Timer 7 Disabled					
6	TER6	R/W	1 = Timer 6 Enabled					
			0 = Timer 6 Disabled					
5	TER5	R/W	1 = Timer 5 Enabled					
			0 = Timer 5 Disabled					
4	TER4	R/W	1 = Timer 4 Enabled					
			0 = Timer 4 Disabled					
3	TER3	R/W	1 = Timer 3 Enabled					
			0 = Timer 3 Disabled					
2	TER2	R/W	1 = Timer 2 Enabled					
			0 = Timer 2 Disabled					
1	TER1	R/W	1 = Timer 1 Enabled					
			0 = Timer 1 Disabled					
0	TER0	R/W	1 = Timer 0 Enabled					
			0 = Timer 0 Disabled					

2.8 Interrupt Flag Registers (TIFR, EIFR, UIFR)

TIER, EIER, and UIER are the interrupt enable registers. Reading an IER register reads its contents and puts the value on the internal data bus. Writing an IER writes a value from the data bus into the register. Setting a bit in an IER to "1" permits the interrupt corresponding to the same bit in the IFR to cause a processor interrupt. If a WAI instruction has been executed prior to the interrupt occurring and the part is in the non-emulation mode (BCR3=0). The RUN pin will be low until the interrupt occurs and will then go high to indicate the part is running.

Note that the "I" flag in the microprocessor status register must be cleared with an instruction before any of the interrupts controlled by TIER, EIER, and UIER can occur.

A bit of these registers is set to a "1" in response to an interrupt signal from a source. Sources specified as level-triggered assert the corresponding IFR bit if an edge occurs and is held to a "1" as long as the IRQB input is held low. Sources specified as edge-triggered assert the corresponding IFR bit upon and only upon transition to the specified polarity. Note that changes for edge-triggered bits are asynchronous with PHI2.

A read from an IFR register transfers its value to the internal data bus.

Write to an IFR register. A write of a "1" to any bits of these registers clears those bits but has no further effect when execution of that write instruction is completed; that is, the bit is reset by a pulse but not held reset. A write of a "0" to any bits of these registers has no effect. Note that you must write a "1" to the corresponding IFR bit after the interrupt has been serviced; otherwise, the interrupt will continue to occur.

Interrupt Priority. If more than one bit of the Interrupt Flag Registers are set to a "1" and enabled, the vector corresponding to the highest memory map location and bit number asserted is used. For example, if both the TIFR1 and EIFR3 were asserted and enabled, then the vector corresponding to EIFR3 would be used. For another example, if both the TIFR3 and EIFR0 were asserted and enabled, then the vector corresponding to EIFR0 would be used.

2.8.1 Timer Interrupt Enable Register (TIER) Description

Address = 0xDF46		TIER: Timer Interrupt Enable Register					Reset Value = 0x00	
7:0->	TIER7	TIER6	TIER5	TIER4	TIER3	TIER2	TIER1	TIER0
Bit	**Name**	**Access**	**Description**					
7	TIER7	R/W	1 = Timer 7 Enabled					
			0 = Timer 7 Disabled					
6	TIER6	R/W	1 = Timer 6 Enabled					
			0 = Timer 6 Disabled					
5	TIER5	R/W	1 = Timer 5 Enabled					
			0 = Timer 5 Disabled					
4	TIER4	R/W	1 = Timer 4 Enabled					
			0 = Timer 4 Disabled					
3	TIER3	R/W	1 = Timer 3 Enabled					
			0 = Timer 3 Disabled					
2	TIER2	R/W	1 = Timer 2 Enabled					
			0 = Timer 2 Disabled					
1	TIER1	R/W	1 = Timer 1 Enabled					
			0 = Timer 1 Disabled					
0	TIER0	R/W	1 = Timer 0 Enabled					
			0 = Timer 0 Disabled					

2.8.2 Timer Interrupt Flag Register (TIFR) Description

Address = 0xDF44			TIER: Timer Interrupt Flag Register				Reset Value = 0x00	
7:0->	TIFR7	TIFR6	TIFR5	TIFR4	TIFR3	TIFR2	TIFR1	TIFR0
Bit	**Name**	**Access**	**Description**					
7	TIFR7	R/ W=1 Clears	1 = Timer 7 Interrupted					
			0 = Timer 7 Did not interrupt					
6	TIFR6	R/ W=1 Clears	1 = Timer 6 Interrupted					
			0 = Timer 6 Did not interrupt					
5	TIFR5	R/ W=1 Clears	1 = Timer 5 Interrupted					
			0 = Timer 5 Did not interrupt					
4	TIFR4	R/ W=1 Clears	1 = Timer 4 Interrupted					
			0 = Timer 4 Did not interrupt					
3	TIFR3	R/ W=1 Clears	1 = Timer 3 Interrupted					
			0 = Timer 3 Did not interrupt					
2	TIFR2	R/ W=1 Clears	1 = Timer 2 Interrupted					
			0 = Timer 2 Did not interrupt					
1	TIFR1	R/ W=1 Clears	1 = Timer 1 Interrupted					
			0 = Timer 1 Did not interrupt					
0	TIFR0	R/ W=1 Clears	1 = Timer 0 Interrupted					
			0 = Timer 0 Did not interrupt					

2.8.3 Edge Interrupt Enable Register (EIER) Description

Address = 0xDF45		TIER: Edge Interrupt Enable Register					Reset Value = 0x00	
7:0->	IRQBE	PIBE	NE66E	NE64E	PWME	PE60E	NE57E	PE56E
Bit	Name	Access	Description					
7	IRQBE	R/W	1 = Enable					
			0 = Disable					
6	PIBE	R/W	1 = Enable					
			0 = Disable					
5	NE66E	R/W	1 = Enable					
			0 = Disable					
4	NE64E	R/W	1 = Enable					
			0 = Disable					
3	PWME	R/W	1 = Enable					
			0 = Disable					
2	PE60E	R/W	1 = Enable					
			0 = Disable					
1	NE57E	R/W	1 = Enable					
			0 = Disable					
0	PE56E	R/W	1 = Enable					
			0 = Disable					

2.8.4 Edge Interrupt Flag Register (EIFR) Description

Address = 0xDF47	EIER: Edge Interrupt Flag Register						Reset Value = 0x00	
7:0->	IRQB	PIB	NE66	NE64	PWM	PE60	NE57	PE56
Bit	Name	Access	Description					
7	IRQB	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
6	PIB	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
5	NE66	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
4	NE64	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
3	PWM	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
2	PE60	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
1	NE57	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					
0	PE56	R/ W=1 Clears	1 = Interrupted					
			0 = Did not interrupt					

2.8.5 UART Interrupt Enable Register (UIER) Description

Address = 0xDF49			UIER: UART Interrupt Enable Register					Reset Value = 0x00	
7:0->	U3TE	U3RE	U2TE	U2RE	U1TE	U1RE	U0TE	U0RE	
Bit	**Name**	**Access**	**Description**						
7	U3TE	R/W	1 = Enable						
			0 = Disable						
6	U3RE	R/W	1 = Enable						
			0 = Disable						
5	U2TE	R/W	1 = Enable						
			0 = Disable						
4	U2RE	R/W	1 = Enable						
			0 = Disable						
3	U1TE	R/W	1 = Enable						
			0 = Disable						
2	U1RE	R/W	1 = Enable						
			0 = Disable						
1	U0TE	R/W	1 = Enable						
			0 = Disable						
0	U0RE	R/W	1 = Enable						
			0 = Disable						

2.8.6 UART Interrupt Flag Register (UIFR) Description

Address = 0xDF47	UIFR: UART Interrupt Flag Register						Reset Value = 0x00	
7:0->	IRQATx	U3RE	IRQATx	U2RE	IRQATx	U1RE	IRQATx	U0RE
Bit	**Name**	**Access**	**Description**					
7	IRQATx	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
6	U3RF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
5	U2TF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
4	U2RF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
3	U1TF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
2	U1RF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
1	U0TF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					
0	U0RF	R/ W=1 Clears	1 = Interrupted 0 = Did not interrupt					

2.9 Universal Asynchronous Receiver/Transmitters (UARTs)

The W65C265S has four full duplex Universal Asynchronous Receiver/Transmitters (UART) with programmable bit rates. The serial I/O functions are controlled by the Asynchronous Communication Control and Status Registers (ACSRx). The serial bit rate is determined by Timer 3 or 4 for all modes for the UART's. The maximum data rate using the internal clock is 0.5MHz bits per second (FCLK = 8MHz). The Asynchronous Transmitter and Asynchronous Receiver can be independently enabled or disabled.

All transmitter and receiver bit rates will occur at one sixteenth of Timer 3 or 4 as selected.

Whenever Timer 3 or 4 is required as a timing source, it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Table 1-3 for a table of hexadecimal values that represent the desired data rate.

Standard UART Features

- 7 or 8 bit data with or without Odd or Even parity.
- The Transmitter has 1 stop bit with parity or 2 stop bits without parity.
- The Receiver requires only 1 stop bit for all modes.
- Both the Receiver and Transmitter have priority encoded interrupts for service routines.
- The Receiver has error detection for parity error, framing error, or over-run error conditions that may require re-transmission of the message.
- The Receiver Interrupt occurs due to a receiver data register full condition.
- The Transmitter Interrupt can be selected to occur on either the data register empty (end-of-byte transmission) or both the data register empty and the shift register empty (end-of-message transmission) condition.
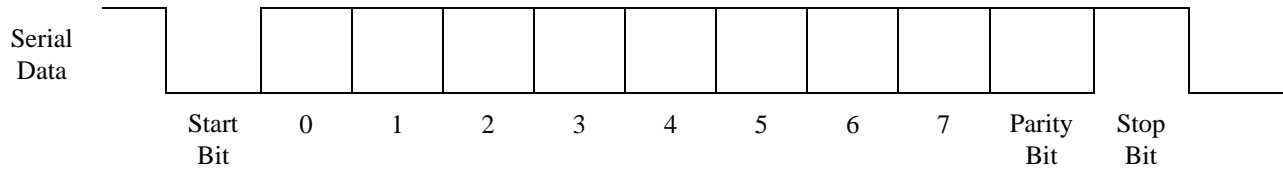
2.9.1 Transmitter Operation

The transmitter operation is controlled by the Asynchronous Control and Status Register (ACSRx. The transmitter automatically adds a start bit, parity bit and one or two stop bits as defined by the ACSRx. A word of transmitted data is 7 or 8 bits of data.

The Transmitter Data Register (ARTDx) is located at addresses $DF71, $DF73, $DF75, and $DF77 and is loaded on a write. The Receiver is read at this same address.

2.9.2 UART Data Register Description

Address = Base + 1		ARTDx: UART Data Register					Reset Value = 0x00	
7:0->	ARTDx7	ARTDx6	ARTDx5	ARTDx4	ARTDx3	ARTDx2	ARTDx1	ARTDx0
Bit	Name	Access	Description					
7 - 0	**ARTDx** [7-0]	R/W	R = Read Receiver Data Register					
			W = Write Transmitter Data Register					

Serial
Data

| Start Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Parity Bit | Stop Bit |

2.9.3 Transmitter Mode with Parity

The Transmitter Interrupt is controlled by the Asynchronous Control Status Register bit ACSRx1.

IRQATx = ACSRx0 ((ACSRx1B) (DATA REGISTER EMPTY) + (ACSRx1) (DATA REGISTER AND SHIFT REGISTER EMPTY))

2.9.4 Receiver Operation

The receiver and its selected control and status functions are enabled when ACSRx5 is set to a "1". The data format must have a start bit, 7 or 8 data bits, and one stop bit or one parity bit and one stop bit. The receiver bit period is divided into 16 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit, and a strobe signal is generated at the approximate center of each incoming bit. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. A framing error, parity error or an over-run will set ASCRx7 the receiver error detection bit. An over-run condition occurs when the receiver data register has not been read and new data byte is transferred from the receiver shift register.

Serial
Data

| Start Bit | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Stop Bit | Stop Bit |
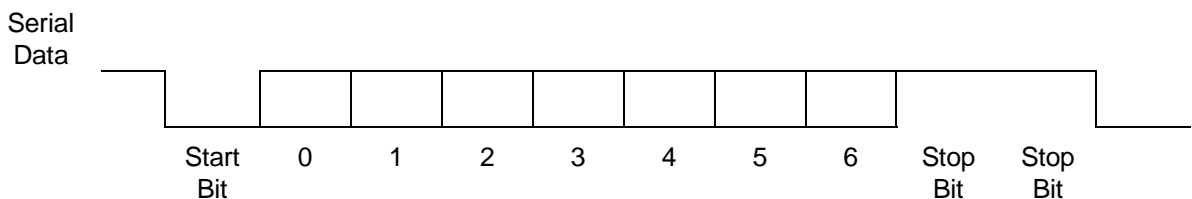
2.9.5 Data Timing for 7-bit Data without Parity and two stop bits.

The receiver requires only one stop bit but the transmitter supplies two stop bits for older system timing.

A receiver interrupt (IRQARx) is generated whenever the receiver shift register is transferred to the receiver data register.

2.9.6 UART RXD and TXD Data Rate Generation

Timer 3 and 4 provide clock timing for the RXD and TXD data rate. Timer 3 and 4 operate as configured by Timer Control Register (TCRx) and Timer Enable Register (TERx) should be set up prior to enabling the UARTx.

The table below identifies the values to be loaded into Timer 3 and 4 to select standard data rates. Any data rate can be selected by using the formula:

$$N = (FCLK / (16 \times bps)) - 1$$

N = decimal value to be loaded into timer using its hexadecimal equivalent
FCLK = the clock frequency
Bps = the desired data rate

Note that one may notice slight differences between the standard rate and the actual data rate. However, transmitter and receiver error of 1.5% or less is acceptable.

Table 2.9.6-1 Timer 3 and 4 Values for Baud Rate Selection

Standard Baud Rate	1.8432MHz	2.4576MHz	3.6864MHz	4.9152MHz	6.1440MHz
110	$0416	$0573	$082E	$0AE8	$0DA2
150	$02FF	$03FF	$05FF	$07FF	$09FF
300	$017F	$01FF	$02FF	$03FF	$04FF
600	$00BF	$00FF	$017F	$01FF	$027F
1200	$005F	$007F	$00BF	$00FF	$013F
1800	$003F	$0054	$007F	$00AA	$00DF
2400	$002F	$003F	$005F	$007F	$009F
4800	$0017	$001F	$002F	$003F	$004F
9600	$000B	$000F	$0017	$001F	$0027
19200	$0005	$0007	$000B	$000F	$0013
38400	$0002	$0003	$0005	$0007	$0009
57600	$0001	$0002	$0003	$0004	$0006

Note: Shading indicates transmitter or receiver error greater than 1.5%.

2.9.7 Asynchronous Control and Status Registers (ACSRx) Description

The Asynchronous Control and Status Register (ACSRx) enables the Receiver and Transmitter and holds information on communication status error conditions.

Address = Base			ACSRx: Asynchronous Control and Status Register				Reset Value = 0x00	
7:0->	ACSRx7	ACSRx6	ACSRx5	ACSRx4	ACSRx3	ACSRx2	ACSRx1	ACSRx0
Bit	Name	Access	Description					
7	ACSRx7	R/W	1 = <u>Receiver Error Flag</u>. The Receiver logic detects three possible error conditions and sets ACSRx7: parity, framing or over-run. A parity error occurs when the parity bit received does not match the parity generated on the receive data. A framing error occurs when the stop bit time finds a "0" instead of a "1". An over-run occurs when the last data in the Receiver Data Register has not been read and new data is transferred from the Receive Shift Register.					
			0 = Cleared by writing a "1" to ACSRx7. Writing a "0" to ACSR7 has not effect on ACSRx7.					
6	ACSRx6	R/W	1 = Software Semaphore. ACSRx6 may be used for communications among routines which access the UARTx. This bit has no effect on the UART operation. The bit can be thought of as a manually set busy signal.					
			0 = User defined.					
5	ACSRx5	R/W	1 = Enable Receiver, Receiver Interrupt, and RXDx output on Port 6.					
			0 = Disable Receiver.					
4	ACSRx4	R/W	1 = Even parity is enabled. Even parity is when the number of ones in the data register plus parity bit equal an even number of "1's".					
			0 = Odd parity is enabled. Odd parity is generated where the number of ones is the data register plus parity bit equal an odd number of "1's".					
3	ACSRx3	R/W	1 = Enable Parity.					
			0 = Disable Parity					
2	ACSRx2	R/W	1 = Transmitter and Receiver send and receive 8-bit data. The Transmitter sends 11 bits of information (one start, 8 data, one parity and one stop or two stop bits). The Receiver receives 10 or 11 bits of information (one start, 8 data, one stop or one parity and one stop bit).					
			0 = Transmitter and Receiver send and receive 7-bit data. The Transmitter sends a total of 10 bits of information (one start, 7 data, one parity and one stop or 2 stop bits). The Receiver receives 9 or 10 bits of information (one start, 7 data, and one stop or one stop and one parity bits). When writing to the Transmitter in seven bit mode, bit 7 is discarded. When reading from the receive data register during seven bit mode, bit 7 is always zero.					
1	ACSRx1	R/W	1 = Transmitter Interrupt occurs due to both the Transmitter Data and Shift register empty condition (end-of-message transmission. ACSRx0 = 0 clears this bit if set.					
			0 = Transmitter Interrupt occurs due to a Transmitter Data Register Empty condition (end-of-byte transmission).					
0	ACSRx0	R/W	1 = Enable Transmitter,Transmitter Interrupt, and TXDx on Port 6					
			0 = Disable Transmitter,Transmitter Interrupt, and TXDx on Port 6					

2.10 Parallel Interface Bus (PIB)

The Parallel Interface Bus (PIB) is used to communicate instructions and data to and from task oriented processors, smart peripherals, co-processors, and parallel processors.

Register 3 may have a primary role of communicating commands or opcodes between processors.

Register 7 may have a primary role of communicating data or addresses between processors.

PIRS 2,1,0 Register Address		
111	0xDF7F	PIR7 (Automatic Handshake)
110	0xDF7E	PIR6
101	0xDF7D	PIR5
100	0xDF7C	PIR4

011	0xDF7B	PIR3 (Automatic Handshake)
010	0xDF7A	PIR2

001	0xDF79	PIBER (PIB Enable Register)
000	0xDF78	PIBFR (PIB Flag Register)

Figure 2.10-1 PIB Registers

Address = Base + 2-7		PIR2-7: Parallel Interface Registers 2-7					Reset Value = xx	
7:0->	PIRx7	PIRx6	PIRx5	PIRx4	PIRx3	PIRx2	PIRx1	PIRx0
Bit	Name	Access	Description					
7 - 0	**PIRx**[7-0]	R/W	R = Read by Processor and Host					
			W = Write by Processor and Host					

2.10.1 PIB Enable Register (PIBER) Description

Address = 0xDF79	PIBER: PIB Interrupt Enable Register					Reset Value = 0x00	
7:0->	PIBER7	PIBER6	PIBER5	PIBER4	PIBER3	PIBER2	PIBER1	PIBER0
Bit	**Name**	**Access**	**Description**					
7	PIBER7	R/W	1 = Enable Automatic Handshake Input Data in PIR7 Interrupt *3					
			0 = Disable *3					
6	PIBER6	R/W	1 = Enable Automatic Handshake Output Data in PIR7 Interrupt *2					
			0 = Disable *2					
5	PIBER5	R/W	1 = Enable Manual Handshake from Host *3					
			0 = Disable *3					
4	PIBER4	R/W	1 = Enable Manual Handshake from Processor *2					
			0 = Disable *2					
3	PIBER3	R/W	1 = Enable Automatic Handshake Input Data in PIR3 Interrupt *3					
			0 = Disable *3					
2	PIBER2	R/W	1 = Enable Automatic Handshake Output Data in PIR3 Interrupt *2					
			0 = Disable *2					
1	PIBER1	R/W	1 = Enable RDB and WRB *3					
			0 = Disable *3					
0	PIBER0	R/W	1 = Enable PIB *3					
			0 = Disable PIB *3					

Notes:
*1 Read only from Host or Processor
*2 Read only from Processor, Read or Write from Host
*3 Read only from Host, Read or Write from Processor
*4 Read only from Host or Processor, will always read back a zero.

2.10.2 PIB Flag Register (PIBFR) Description

Address = 0xDF78	PIBFR: Timer Interrupt Flag Register						Reset Value = 0x00	
7:0->	PIBFR7	PIBFR6	PIBFR5	PIBFR4	PIBFR3	PIBFR2	PIBFR1	PIBFR0
Bit	**Name**	**Access**	**Description**					
7	PIBFR7	R/W	1 = Host Write to PIR7 and Interrupt Processor *1					
			0 = Cleared by Processor Read of PIR7 *1					
6	PIBFR6	R/W	1 = Processor Write to PIR7 and Interrupt Host *1					
			0 = Cleared by Host Read of PIR7 *1					
5	PIBFR5	R/W	1 = Write "1" from Host and Interrupt Processor *2					
			0 = Write "0" from Host *2					
4	PIBFR4	R/W	1 = Write "1" from Processor and Interrupt Host *3					
			0 = Write "0" from Processor *3					
3	PIBFR3	R/W	1 = Host Write to PIR3 and Interrupt Processor *1					
			0 = Processor Read of PIR3 *1					
2	PIBFR2	R/W	1 = Processor Write to PIR3 and Interrupt Host *1					
			0 = Host Read of PIR3 *1					
1	PIBFR1	R/W	1 = Enable RDB and WRB *4					
			0 = Disable *4					
0	PIBFR0	R/W	1 = Enable P4B *4					
			0 = Disable P4B *4					

Notes:
*1 Read only from Host or Processor
*2 Read only from Processor, Read or Write from Host
*3 Read only from Host, Read or Write from Processor
*4 Read only from Host or Processor, will always read back a zero.

2.11 Twin Tone Generators

Each Tone Generator (TGx), as shown in figure 1-13 is comprised of a 16 bit timer and a 16 step divider circuit that selects the proper Digital to Analog (DA) output level. The enable bits for the tone generators are located in bits 1 and 2 of the BCR register.

DA Level n = E COS (π x (2n+1) /16) $0 \leq n \leq 7$
N = value loaded into timer latches
Register Value N = (FCLK / (16 x F)) - 1
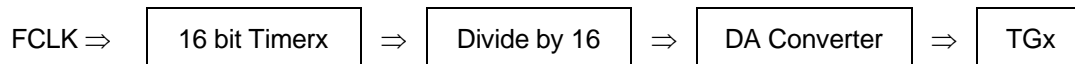F=desired frequency
FCLK = FCLK input clock

FCLK $\Rightarrow$ | 16 bit Timerx | $\Rightarrow$ | Divide by 16 | $\Rightarrow$ | DA Converter | $\Rightarrow$ | TGx |

Figure 2.11-1 Tone Generator Block Diagram

| | Oscillator FCLK = 3.579545 MHz | | | | Oscillator FCLK = 4.000000 MHz | | |
| | Standard Frequency (Hz) | Register Value | | Actual Frequency (Hz) | Register Value | | Actual Frequency (Hz) |
		Hexa-decimal	Decimal		Hexa-decimal	Decimal	
DTMF Row	697	0140	320	697	0166	358	696
	770	0122	290	769	0144	324	769
	852	0106	262	851	0124	292	853
	941	00ED	237	940	0109	265	940
DTMF Column	1209	00B8	184	1209	00CE	206	1208
	1336	00A6	166	1340	00BA	186	1337
	1477	0096	150	1482	00AB	168	1479
	1633	0088	136	1633	0098	152	1634
Subscriber Tones	350	027E	638	350	02C9	713	350
	440	01FB	507	440	0237	567	440
	480	01D1	465	480	0208	520	480
	620	0168	360	620	0192	402	620
US 110, 300 Baud Modem	1070	00D0	208	1070	00E9	233	1068
	1270	00AF	175	1271	00C4	196	1269
	2025	006D	109	2034	007A	122	2033
	2225	0064	100	2215	006F	111	2232
European 110, 300 Baud Modem	980	00E3	227	981	00FE	254	980
	1180	00BD	189	1177	00D3	211	1179
	1650	0087	135	1645	0097	151	1645
	1850	0078	120	1849	0086	134	1832
Teletext	390	023D	573	390	0280	640	390
	450	01F0	496	450	022B	555	450
	1300	00AB	171	1301	00BF	191	1302
	2100	006A	106	2091	0076	118	2101
US 1200 Baud Modem	390	023D	573	390	0280	640	390
	450	01F0	496	450	022B	555	450
	1200	00B9	185	1203	00CF	207	1202
	2200	0065	101	2193	0071	113	2193

Table 2.11-2 Communications Frequencies Generated by the Tone Generator Timers 5 and 6

2.12 **System Speed Control Register (SSCR)**

The System Speed Control Register (SSCR) provides a slowing of the memory clock rate for slower memory. When slower memories are addressed, the PHI2 clock rate is slowed by extending the PHI2 low and high times.

2.12.1 System Speed Control Register (SSCR)

| Address = 0xDF41	SSCR: System Speed Control Register					Reset Value = 0x00	
7:0->	SSCR7	SSCR6	SSCR5	SSCR4	SSCR3	SSCR2	SSCR1	SSCR0
Bit	Name	Access	Description				
7	SSCR7	R/W	1 = CS7 Speed Select = Fast (FCLK)				
			0 = CS7 Speed Select = Slow (FCLK/4)				
6	SSCR6	R/W	1 = CS6 Speed Select = Fast (FCLK)				
			0 = CS6 Speed Select = Slow (FCLK/4)				
5	SSCR5	R/W	1 = CS5 Speed Select = Fast (FCLK)				
			0 = CS5 Speed Select = Slow (FCLK/4)				
4	SSCR4	R/W	1 = CS4 Speed Select = Fast (FCLK)				
			0 = CS4 Speed Select = Slow (FCLK/4)				
3	SSCR3	R/W	1 = System (CS0B-CS7B) Speed Select = Fast (FCLK)				
			0 = System (CS0B-CS7B) Speed Select = Slow (FCLK/4)				
2	SSCR2	R/W	1 = External RAM 0x0000-01FF				
			0 = Internal RAM 0x0000-01FF				
1	SSCR1	R/W	1 = PHI2 clock source is FCLK/4 or FCLK				
			0 = PHI2 clock source is CLK				
0	SSCR0	R/W	1 = Start FCLK				
			0 = Stop FCLK				
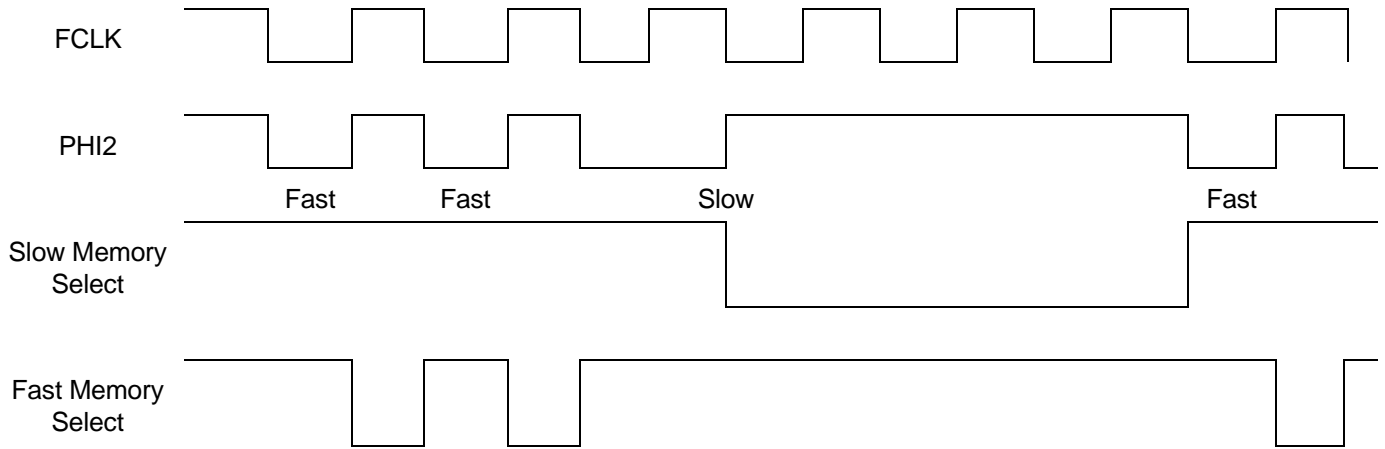
Figure 2.12.1-1 System Speed Change Timing Diagram

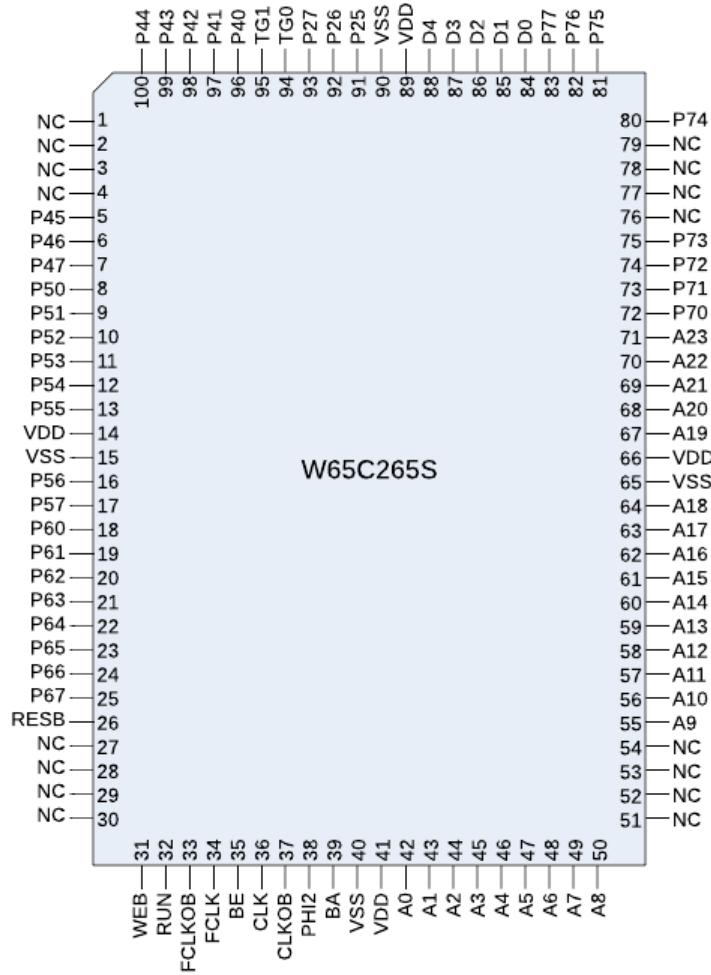# 3 Pin and Pin Function Description for 84 Pin PLCC

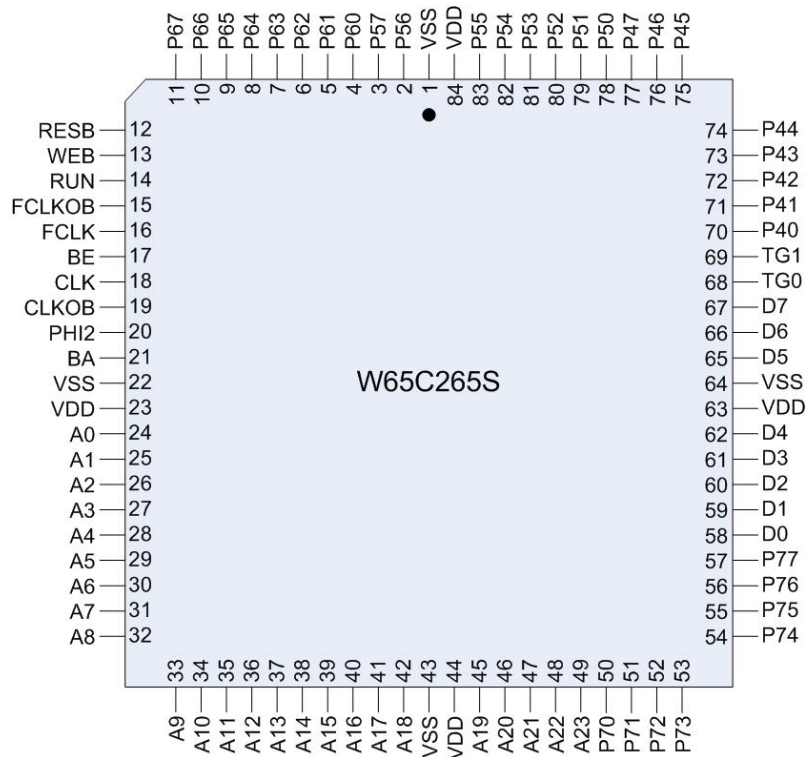**Figure 2-2a 100 Lead QFP Chip Carrier Pinout**

Figure 2-2b 84 Lead Chip Carrier Pinout
Note: This PLCC package is only available in limited quantities.
Use QFP100 package for new designs.

PLCC 84 Pin	QFP 100 Pin	Name	Control Bit	Signal with Control Bit=0	Signal with Control Bit=1
1	15	VSS	---	VSS	VSS
2	16	P56	EIER0	P56	PE56
		PID6	PIBER0		PID6
3	17	P57	EIER1	P57	NE57
		PID7	PIBER0		PID7
4	18	P60	ACSR05	P60	RXD0
		TIN	TCR1		TIN
		PE60	EIER02	P60	PE60
5	19	P61	ACSR00	P61	TXD0
		TOUT	TCR0		TOUT
6	20	P62	ACSR15	P62	RXD1
		PWM	TCR2+TCR3		PWM
7	21	P63	ACSR10	P63	TXD1
		TOUT			
8	22	P64	ACSR25	P64	RXD2
		NE64	EIER4	P64	NE64
9	23	P65	ACSR20	P65	TXD2
10	24	P66	ACSR35	P66	RXD3
		NE66	EIER5	P66	NE66
11	25	P67	ACSR30	P67	TXD3
12	26	RESB	---	RESB	RESB
13	31	WEB	---	WEB	WEB
14	32	RUN	BCR3	RUN	RUN
15	33	FCLKOB	---	FCLKOB	FCLKOB
16	34	FCLK	---	FCLK	FCLK
17	35	BE	---	BE	BE
18	36	CLK	---	CLK	CLK
19	37	CLKOB	---	CLKOB	CLKOB
20	38	PHI2	---	PHI2	PHI2
21	39	BA	BCR3	BA/1	BA
22	40	VSS	---	VSS	VSS
23	41	VDD	---	VDD	VDD

24	42	A0	BCR0	P00	A0
25	43	A1	BCR0	P01	A1
26	44	A2	BCR0	P02	A2
27	45	A3	BCRO	PO3	A3
28	46	A4	BCR0	P04	A4
29	47	A5	BCR0	P05	A5
30	48	A6	BCR0	P06	A6
31	49	A7	BCR0	P07	A7
32	50	A8	BCR0	P10	A8
33	55	A9	BCR0	P11	A9
34	56	A10	BCR0	P12	A10
35	57	A11	BCR0	P13	A11
36	58	A12	BCR0	P14	A12
37	59	A13	BCR0	P15	A13
38	60	A14	BCR0	P16	A14
39	61	A15	BCR0	P17	A15
40	62	A16	BCR0	P30	A16
41	63	A17	BCR0	P31	A17
42	64	A18	BCR0	P32	A18
43	65	VSS	---	VSS	VSS
44	66	VDD	---	VDD	VDD
45	67	A19	BCR0	P33	A19
46	68	A20	BCR0	P34	A20
47	69	A21	BCR0	P35	A21
48	70	A22	BCR0	P36	A22
49	71	A23	BCR0	P37	A23
50	72	P70	PCS70	P70	CS0B
51	73	P71	PCS71	P71	CS1B
52	74	P72	PCS72	P72	CS2B
53	75	P73	PCS73	P73	CS3B
54	80	P74	PCS74	P74	CS4B
55	81	P75	PCS75	P75	CS5B
56	82	P76	PCS76	P76	CS6B
57	83	P77	PCS77	P77	CS7B

58	84	D0	BCR0	P20	D0
59	85	D1	BCR0	P21	D1
60	86	D2	BCR0	P22	D2
61	87	D3	BCR0	P23	D3
62	88	D4	BCR0	P24	D4
63	89	VDD	---	VDD	VDD
64	90	VSS	---	VSS	VSS
65	91	D5	BCR0	P25	D5
66	92	D6	BCR0	P26	D6
67	93	D7	BCR0	P27	D7
68	94	TG0	TCR31	---	TG0
69	95	TG1	TCR33	---	TG1
70	96	P40	BCR5 · BCR6	P40	NMIB
		ABORTB	BCR5 · BCR6B		ABORTB
71	97	P41	EIER3	P41	IRQB
72	98	P42	PIBER0	P42	PIIB
73	99	P43	PIBER0 · PIBER1B	P43	PIWEB
		PIWRB	PIBER0 · PIBER1		PIWRB
74	100	P44	PIBER0 · PIBER1B	P44	PICSB
		PIRDB	PIBER0 · PIBER1		PIRDB
75	5	P45	PIBER0	P45	PIRS0
76	6	P46	PIBER0	P46	PIRS1
77	7	P47	PIBER0	P47	PIRS2
78	8	P50	PIBER0	P50	PID0
79	9	P51	PIBER0	P51	PID1
80	10	P52	PIBER0	P52	PID2
81	11	P53	PIBER0	P53	PID3
82	12	P54	PIBER0	P54	PID4
83	13	P55	PIBER0	P55	PID5
84	14	VDD	---	VDD	VDD

3.1 Write Enable (active low) (WEB)

The WEB signal is high when the microprocessor is reading data from external memory or I/O and high when it is reading or writing to internal memory or I/O.   When WEB is low the microprocessor is writing to external memory or external I/O. The WEB signal is bi-directional; when BE is low this is an input for DMA operations to on-chip RAM or I/O. When BE is high the internal microprocessor controls WEB.

3.2 RUN and SYNC outputs with WAI and STP defined (RUN)

The RUN function of the RUN output is pulled low as the result of a WAI or STP instruction. RUN is used to signal an external oscillator to start PHI2. The processor is stopped when RUN is low.

When BCR3=1 (emulation mode), the SYNC function (SYNC=1 indicates an opcode fetch) is multiplexed on RUN during PHI2 low time and RUN is multiplexed during PHI2 high time. When BCR3=0 (normal operating mode), the RUN function is output during the entire clock cycle. An ICE system can demultiplex RUN to provide full emulation capability for the RUN function.

The BE input has no effect on RUN.

When RUN goes low the PHI2 signal may be stopped when high or low; however, it is recommended PHI2 stop in the high state. When RUN goes high due to an enabled interrupt or reset, the internal PHI2 clock is requested to start. The clock control function is referred to as the RUN function of RUN.

The WAI instruction pulls RUN low during PHI2 high time. RUN stays low until an enabled interrupt is requested or until RESB goes from low to high, starting the microprocessor.

The STP instruction pulls RUN low during PHI2 high time and stops the internal PHI2 clock. RUN remains low and the clock remains stopped until RESB goes from low to high.

FCLK can be started or stopped by writing to System Speed Control Register (SSCR) bit 0. When SSCR0=0 (reset forces SSCR0=0), FCLK is stopped. When SSCR0=1, FCLK is started. When starting FCLK oscillator, the system software should wait (100 milliseconds or an appropriate amount of time) for the oscillator to be stable before using FCLK.

3.3 Phase 2 Clock Output (PHI2)

PHI2 output is the main system clock used by the microprocessor for instruction timing, general on-chip memory, and I/O timing. The PHI2 clock source is either CLK or FCLK depending on the value of System Speed Control Register bit 1 (SSCR1). When SSCR1=0, then CLK is the PHI2 clock source. When SSCR1=1, then FCLK is the PHI2 clock source.

3.4 Clock Inputs (CLKOB, FCLKOB Outputs) (CLK. FCLK)

CLK and FCLK inputs are used by the timers, for PHI2 system clock generation, counting events or implementing Real Time clock type functions. CLK should always be equal to or less than one-fourth the FCLK clock rate when FCLK is running (see the timer description for more information). CLKOB, FCLKOB outputs are the inverted CLK and FCLK inputs that are used for oscillator circuits that employ crystals or a resistor-capacitor time base.

3.5 Bus Enable and RDY Input (BE)

BE controls the address bus, data bus and WEB signals. When RESB goes high signaling in the power-up condition, the processor starts; and if BE was low when RESB went from low to high then the Bus Control Register (BCR) bits 0, 3, and 7 (BCR0, BCR3, and BCR7) are set to 1 (emulation mode). See Figure 1-1.

After RESB goes high BE controls the direction of the address bus (A0-A7, A8-A15, A16-A23), data bus (D0-D7) and WEB.

When BE goes low during PHI2 low time, the address bus and WEB are inputs, providing for DMA (direct memory and I/O access) for emulation purposes. Data from D0-D7 is written to any register addressed by A0-A15 when WEB is low. Data is read from D0-D7 when WEB is high. The W65C816S is stopped when BE is low, during PHI2 high time.

When BE is high, the A0-A15, D0-D7 and WEB are controlled by the on-chip microprocessor. When BE is pulled low during PHI2 high time, BE does not affect the direction of the address, data BUS and WEB signals. When BE is pulled low in PHI2 high time, the W65C816S is stopped so that the processor may be single stepped in emulation.

Figure 3.5-1 BE Timing Relative to PHI2

$$BE = BE \cdot (RDY + PHI2B)$$
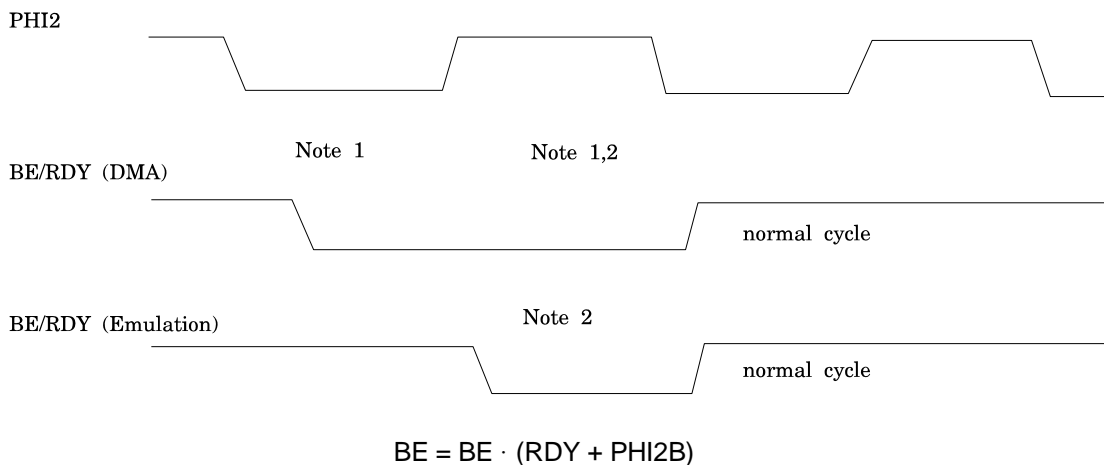
Notes:

1) Address and WEB are inputs with data bus input except when reading on-chip I/O registers or memory. Use this mode for DMA.

2) W65C816S stopped with RDY function of BE pin. When BCR3=1, the W65C816S read or write of internal I/O register or memory is output on the external data bus so that the internal data bus may be traced in emulation.

3.6 Reset Input/Output (active low) (RESB)

When RESB is low for 2 or more processor PHI2 cycles all activity on the chip stops and the chip goes into the static low power state.

After a Reset, all I/O pins become inputs. Because of NOR gates on the inputs, RESB disables all input buffers. The inputs will not float due to the bus holding devices while RESB is low. Inputs that are unaffected by RESB are BE and WEB.

When RESB goes from low to high, RUN goes high, the Bus Control Register is initialized to $89 if BE is low or to $00 if BE is high. The MPU then begins the power-up reset interrupt sequence in which the program counter is loaded with the reset vector that points to the first instruction to be executed. (See WDC's W65C816S microprocessor data sheet for more information and instruction timing.)

The reset sequence takes 9 cycles to complete before loading the first instruction opcode.

RESB is a bidirectional pin which is pulled low internally for "restarting" due to a "monitor time out", Timer M times out causing a system Reset. (See section 1.5, The Timers for more information.)

3.7 Positive Power Supply (VDD)

VDD is the positive power supply and has a range of 2.8V to 5.5V for use in a wide range of applications.

3.8 Internal Logic Ground (VSS)

VSS is the system logic ground. All voltages are referenced to this supply pin.

3.9 I/O Port Pins (Pxx)

All ports, except Port 7, which is an output Port, are bi directional I/O ports. Each of these bi-directional Ports has a port data register (PDx) and port data direction register (PDDx). A zero ("0") in PDDxx defines the associated I/O pin as an input with the output transistors in the "off" high impedance state. A one ("1") in PDDxx defines the I/O pin as an output. A read of PDx always "reads" the pin. After reset, all Port pins become input pins with both the data and data direction registers reset to 0.

Port 7 has a Chip Select register (PCS) that is used to enable Chip Selects (CSxB). A "1" in bit x of PCSx enables Chip Select CSx- to be output over P7x while a "0" in PCSx specifies   the value in the output data register is to be output on P7x. Port 7 data register is set to all "1's" after Reset, and PCS is cleared to all "0's" after Reset.

3.10 Address Bus (Axx)

Ports 0, 1, and 3 are also the address bus A0-A23 when configured by the Bus Control Register (BCR). When BCR0 and BCR7 are set to "1" and BCR3=0 (normal operating mode) for external memory addressing, Axx are all "1's" when addressing on-chip memory. When BCR3=1 (emulation mode), the address bus is always active so that an emulator can trace internal read and write operations.

3.11 Data Bus (Dx)

Port 2 is the data bus D0-D7 when configured by the Bus Control Register (BCR). (See section 1.4 for BCR mode selection.) When BCR0 and BCR7 are set to a "1" and BCR3=0 (normal operating mode) for external memory addressing, Dx are all "1's" when addressing on-chip memory. When BCR3=1 (emulation mode), the data bus is always active so that an emulator can trace internal read and write operations. During external memory cycles the data bus is in the Hi-Z state during PHI2 low time.

3.12 Positive Edge Interrupt inputs (PExx)

Port pin P56, P60 and P62 have Positive Edge sensitive interrupt inputs (PE56,PE60,PWM) multiplexed with the I/O. The associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a positive transition from "0" to "1". The transition from "1" to "0" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is "1", interrupts are disabled.

3.13 Negative Edge Interrupt inputs (NExx)

Port pin P57, P62, P64 and P66 have Negative Edge sensitive interrupt inputs (NE57, PWM, NE64, NE66) multiplexed with the I/O. The associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a negative transition from "1" to "0". The transition from "0" to "1" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is a "1", interrupts are disabled.

3.14 Chip Select outputs (active low) (CSxB)

The CSxB Chip Select outputs are enabled (individually) as outputs on Port 7 with the PCS register. Each of the eight chip selects is dedicated to one block of external memory defined by the programmable chip select registers; the mapping of each chip select to external addresses is given in Table 1-5, System Memory Map.

3.15 Level Sensitive Interrupt Request input (IRQB)

The I/O function of port pin P41 is multiplexed with IRQB Level Sensitive Interrupt input. When IRQB is held low the Edge Interrupt Flag Register Bit 7 (EIFR7) is set to a "1". When the Edge Interrupt Enable Register bit 7 (EIER7) is set to a "1" the MPU will be interrupted provided the I flag of the MPU is cleared to a "0" allowing interrupts. Unlike the edge interrupts, which do not hold the interrupt bit set, an interrupt will be generated as long as IRQB is low.

3.16 Non-Maskable Edge and ABORT Interrupt Input (NMIB/ABORTB)

The I/O Function of port pin P40 is multiplexed with both the NMIB edge triggered interrupt and the ABORT interrupt. When BCR6=1, the NMIB interrupt is enabled; the MPU will be interrupted on all negative edges of NMIB. Because the I flag cannot prevent NMIB from interrupting, NMIB is thought of as Non-Maskable. When BCR5=1, the ABORT interrupt is enabled. Should both BCR5 and BCR6 be set to "1", both NMIB and ABORT are enabled (normally, this is not desirable).

3.17 Asynchronous Receiver Inputs/Transmitter Outputs (RXDx, TXDx)

The W65C265S has four full duplex Universal Asynchronous Receivers and Transmitters (UARTx) that may be enabled by the Asynchronous Control and Status Registers (ACSRs). When a Receiver is enabled by ACSRx0=1 then port pin P60, P62, P64 or P66 becomes the Asynchronous Receiver Input (RXDx). When a Transmitter is enabled by ACSRx4=1, then port pin P61, P63, P65 or P67 becomes the Asynchronous Transmitter Output (TXDx).

3.18 Timer 4 Input and Output (TIN, TOUT)

Timer 4 is controlled by TCRx and TERx. When the UART is not in use, Timer 4 can be used for counting input negative pulses on TIN. Timer 4 can also be used to put out a square wave or rectangular wave form on TOUT. When counting negative pulses on TIN the TIN frequency should always be less than one-half the frequency of PHI2. TOUT changes state on every time-out of Timer 4; therefore, varying waveform and frequency depends on the timer latch values and may be modified under software control. TIN is multiplexed on P60 and TOUT is multiplexed on P61.

2.19 Bus Available/Disable Output Data (BA)

The BA output indicates the microprocessor is using the internal data and address buses when BA is high. The microprocessor is using the external bus when BA is low, then an external device can use the bus without slowing down processing. BE must be used to gain access to the WEB and address bus. When DODB is low (during PHI2 high) then the microprocessor is writing data to the external data bus. The other devices using the bus should disable their outputs. This signal could be thought of as a valid memory address negative edge for sampling the address bus on the negative edge. When BCR3=1(emulation mode) the DODB function is multiplexed on BA during PHI2 high time and BA is multiplexed during PHI2 low time. When BCR3=0 (normal mode) the BA is output during PHI2 low time and a 1 level is output during PHI2 high time.

3.20 Tone Generator Outputs (TGx)

The Twin Tone Generator outputs (TGx) are synthesized 16 step cosine waveform outputs as described in Section 2.21 Twin Tone Generators.

3.21 Parallel Interface Bus (PIB)

The Parallel Interface Bus (PIB) pins are used to communicate between processors in a "star" network configuration or as a co-processor on a "host" processor bus such as an IBM PC or compatible or an Apple II or Mac II personal computer. This PIB may also be used as part of the file server system for large memory systems.

The Parallel Interface Write Enable (PIWEB) input pin is used with the Parallel Interface Chip Select (low active)/Parallel Interface Chip Select (high active) (PICSB/PICS) signal to transfer data to and from the Parallel Interface Register selected by the Parallel Interface Register select (PIRSx) input pins. When PIWEB and PICSB are configured by the Parallel Interface Bus Enable Register bit 1 (PIBER1=0), then the PIB interface is compatible with WDC microprocessor WE- logical operation with the chip select PICSB input. The use of PIWEB and PICS are configured by PIBER1=1.

The PIB interrupt output to the "host" is generated on the Parallel Interface Interrupt (PII) pin. The "host"

interrupt is suggested to be received on the IRQ level interrupt input pin of the "host" processor.

3.22 Pulse Width Measurement Input (PWM)

The Pulse Width Measurement (PWM) input will cause the Timer 7 (T7) counter contents to be transferred to the T7 output latches on the edge(s) selected by the Timer Control Register bits TCR2 and TCR3. The contents of the counter is transferred and an edge interrupt is generated resulting in the EIRF3 being set.

4 TIMING, AC AND DC CHARACTERISTICS

4.1   Absolute Maximum Ratings (Note 1)

Table 4-1 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
Storage Temperature	TS	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1.   Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

4.2 DC Characteristics

VDD = 2.0V to 5.5V (except where noted), VSS = 0V, TA = 0˚C to +70˚C (except where noted)

Table 4-2-1 DC Characteristics

Characteristic	Symbol	Min	Max	Unit
Input High Threshold Voltage CLK, FCLK, RESB, all other inputs	Vih	.9XVDD 0.7XVDD	VDD+0.3 VDD+0.3	V V
Input Low Threshold Voltage CLK, FCLK. RESB, all other inputs	Vil	VSS-0.3 VSS-0.3	.1XVDD .3XVDD	V V
Input Leakage Current (Vin=VSS to VDD, VDD=5.5V) all inputs	Iin	-1	+1	uA
Output High Voltage Ioh=-100uA, VDD=2.8V all outputs	Voh	0.9XVDD	-	V
Output Low Voltage Iol=100uA, VDD-2.8 all outputs	Vol	-	.1XVDD	V
Supply Current (No Load 2.8V and all on-chip 5.5V circuits operating)	Icc	- -	3 6	mA/MHz mA/MHz
Supply Current (No Load) TA=25EC Reset Condition RESB, BE=VSS; CLK=32768 Hz, VDD=5.5V FCLK=HI, PHI2=HI	Ires	-	5	uA
STP Condition CLK=HI, VDD=2.8V FCLK=HI, PHI2=HI	Istp	-	1	uA
Wait for Interrupt Condition CLK=32768 Hz FCLK=HI, VDD=2.8V	Iwai	-	5	uA
Capacitance (sample tested) (Vin=0, Ta=25EC, f=1MHz) all pins except VSS, VDD	Cin	-	10	pF

4.3 AC Characteristics

Table 4.3-1 AC Characteristics

Timing Parameter	Definition
tISA	Address input setup from PHI2
tIHA	Address input hold from PHI2
tODA	Address output delay from PHI2
tOHA	Address output hold from PHI2
tISD	Data input setup from PHI2
tIHD	Data input hold from PHI2
tODD	Data output delay from PHI2
tOHD	Data output hold from PHI2
tISB	BE input setup from PHI2
tIHB	BE input hold from PHI2
tODSY	SYNC output delay from PHI2
tISRR	RDY/RESB input setup from PHI2
tIHRR	RDY/RESB input hold from PHI2
tODRN	RUN output delay from PHI2
tOHRN	RUN output hold from PHI2
tISP	Port input setup from PHI2
tIHP	Port input hold from PHI2
tODP	Port output delay from PHI2
tOHP	Port output hold from PHI2
tISI	Interrupt input setup from PHI2
tIHI	Interrupt input hold from PHI2
tISU	UART Data input setup from PHI2
tIHU	UART Data input hold from PHI2
tODU	UART Data output delay from PHI2
tOHU	UART Data output hold from PHI2
tODD (DMA)	Data output delay from PHI2 (ROM read)
tODPH	PHI2 output delay from CLK/FCLK
tODCSR	CS output delay from PHI2 rising
tODCSF	CS output delay from PHI2 falling
tR	FCLK/CLK rise time
tF	FCLK/CLK fall time
tBR	BE to RESB
tBV	BE to D0-7, A0-15, WEB Valid
CEXT	External Capacitive load
tCYC	CLK cycle time
tPWL	CLK low time
tPWH	CLK high time
tCYC2	PHI2 cycle time
tPWL2	PHI2 low time
tPWH2	PHI2 high time
tCYCF	FCLK cycle time
tPWLF	FCLK low time
tPWHF	FCLK high time

4.4 AC Parameters

Table 4.4-1 AC Parameters

Timing Parameter	VDD=2.8V 1 MHz		VDD=5V+/-10% 8MHz		Units
	Min	Max	Min	Max	
tISA	460	-	22	-	nS
tIHA	20	-	20	-	nS
tODA	-	280	-	90	nS
tOHA	20	-	10	-	nS
tISD	270	-	25	-	nS
tIHD	20	-	15	-	nS
tODD	-	330	-	85	nS
tOHD	10	-	0	-	nS
tISB	390	-	85	-	nS
tIHB	20	-	20	-	nS
tODSY	-	270	-	110	nS
tISRR	430	-	55	-	nS
tIHRR	20	-	20	-	nS
tODRN	-	330	-	110	nS
tOHRN	20	-	20	-	nS
tISP	270	-	60	-	nS
tIHP	20	-	20	-	nS
tODP	-	280	-	90	nS
tOHP	20	-	20	-	nS
tISI	80	-	25	-	nS
tIHI	20	-	20	-	nS
tISU	80	-	60	-	nS
tIHU	20	-	20	-	nS
tODU	-	300	-	90	nS
tOHU	10	-	10	-	nS
tODPH	-	200	-	35	nS
tODCSR	0	100	0	50	nS
tODCSF	0	100	0	50	nS
tR	-	25	-	15	nS
tF	-	25	-	15	nS
tBR	200	-	100	-	nS
tBV	-	190	-	30	nS
CEXT	50	-	50	-	pF
tCYC	4000	inf.	1000	-	nS
tPWL	2000	inf.	500	inf.	nS
tPWH	2000	inf.	500	inf.	nS
tCYC2	TCYCF	inf.	TCYCF	inf.	nS
tPWL2	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tPWH2	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tCYCF	1000	inf.	250	inf.	nS
tPWLF	500	inf.	125	inf.	nS
tPWHF	500	inf.	125	inf.	nS

4.5 AC Timing Diagram Notes

1. tCYC must always be equal to or greater than four times tCYCF when FCLK is running.

2. Rise and Fall Times for all signals are measured on a sample basis from .3xVDD to .7xVDD.

The Rise and Fall times are not programmable on the automated test system that is used for production testing. A typical Rise and Fall time is 5-10ns; therefore, the spec indicates the duty cycle of the clock as tested (tPWL=tCYC/2-tF).

The Rise and Fall times of indicate output Rise and Fall times. The most critical Rise and Fall times are for PHI2 because all timing is related to PHI2.

The input Rise and Fall times can affect the input setup time (tIS), output delay time (tOD) and hold time (tH). This must be taken into account in an application. At 2MHz and 4MHz, the worst case input Rise and Fall times may prevent a system from working.

3. Hold Time for all inputs and outputs is relative to the associated clock edge.

4.6 AC Timing Diagrams
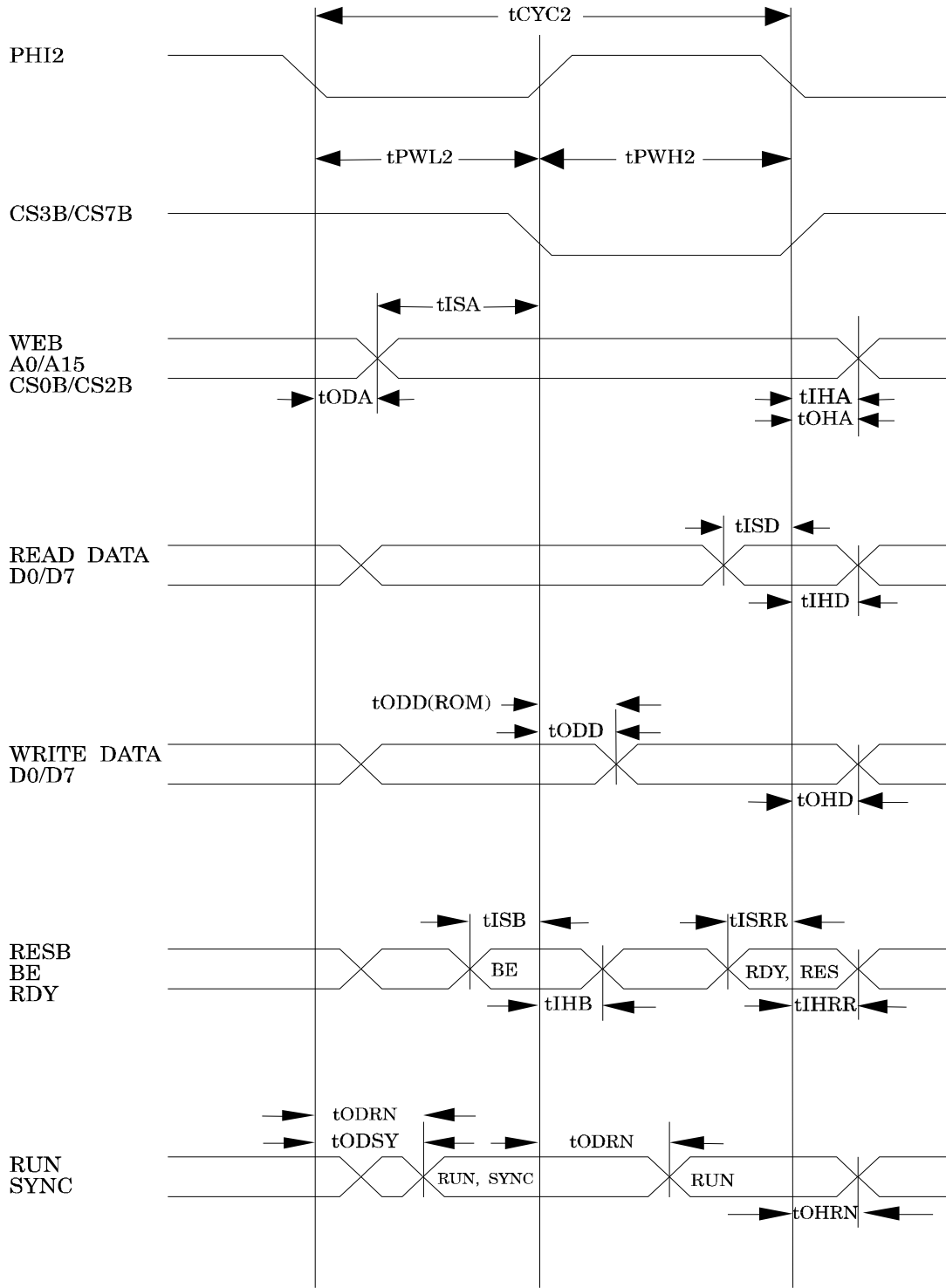
Figure 4.6-1 AC Timing Diagram #1
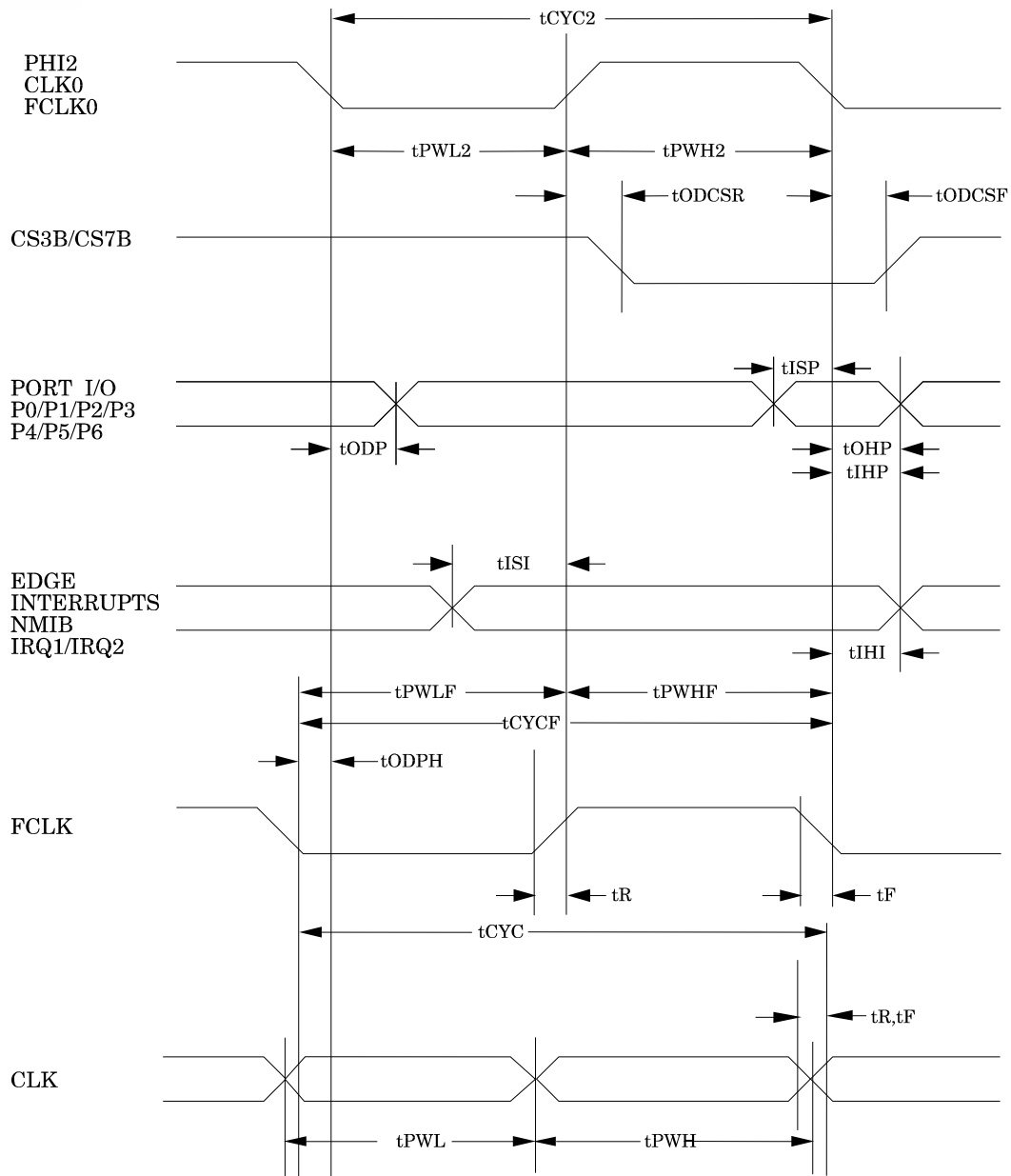
Figure 4.6-2 AC Timing Diagram #2

Notes:
1.   Voltage levels shown are VL = VSS and VH = VDD.
2.   Measurement points shown are .5xVDD and .5xVDD.
3.   CLK can be asynchronous, tCYC equal or greater than 4xtCYCF.
4.   Address and data hold time relative to PHI1 and/or CSxB is 20ns. The PHI2 and CSxB timing is controlled by TCR11. When TCR11=0 PHI12 and CSxB are related to CLK. When TCR11=1, PHI2 and CSxB are related to FCLK.
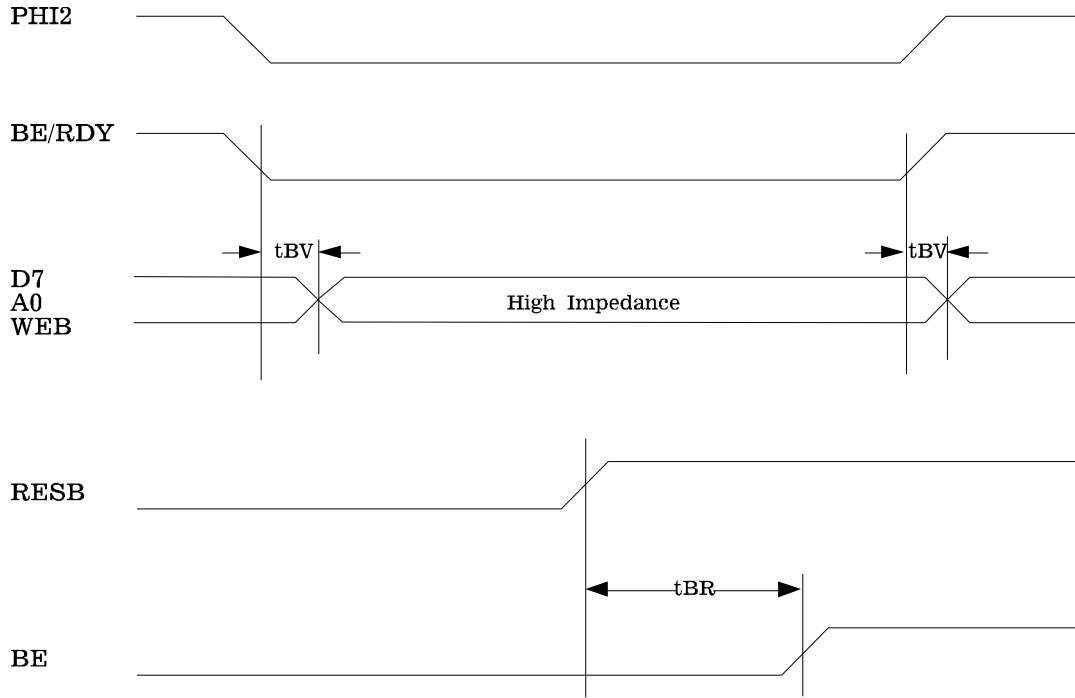
Figure 4.6-3 AC Timing Diagram #3
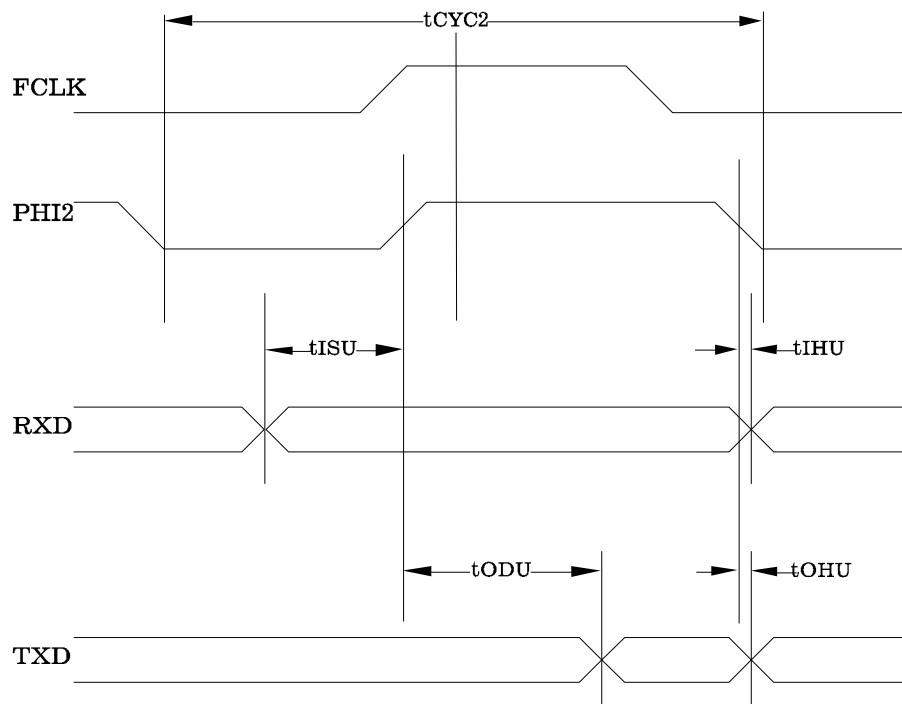
Figure 4.6-4 AC Timing Diagram #4

5 APPLICATION INFORMATION
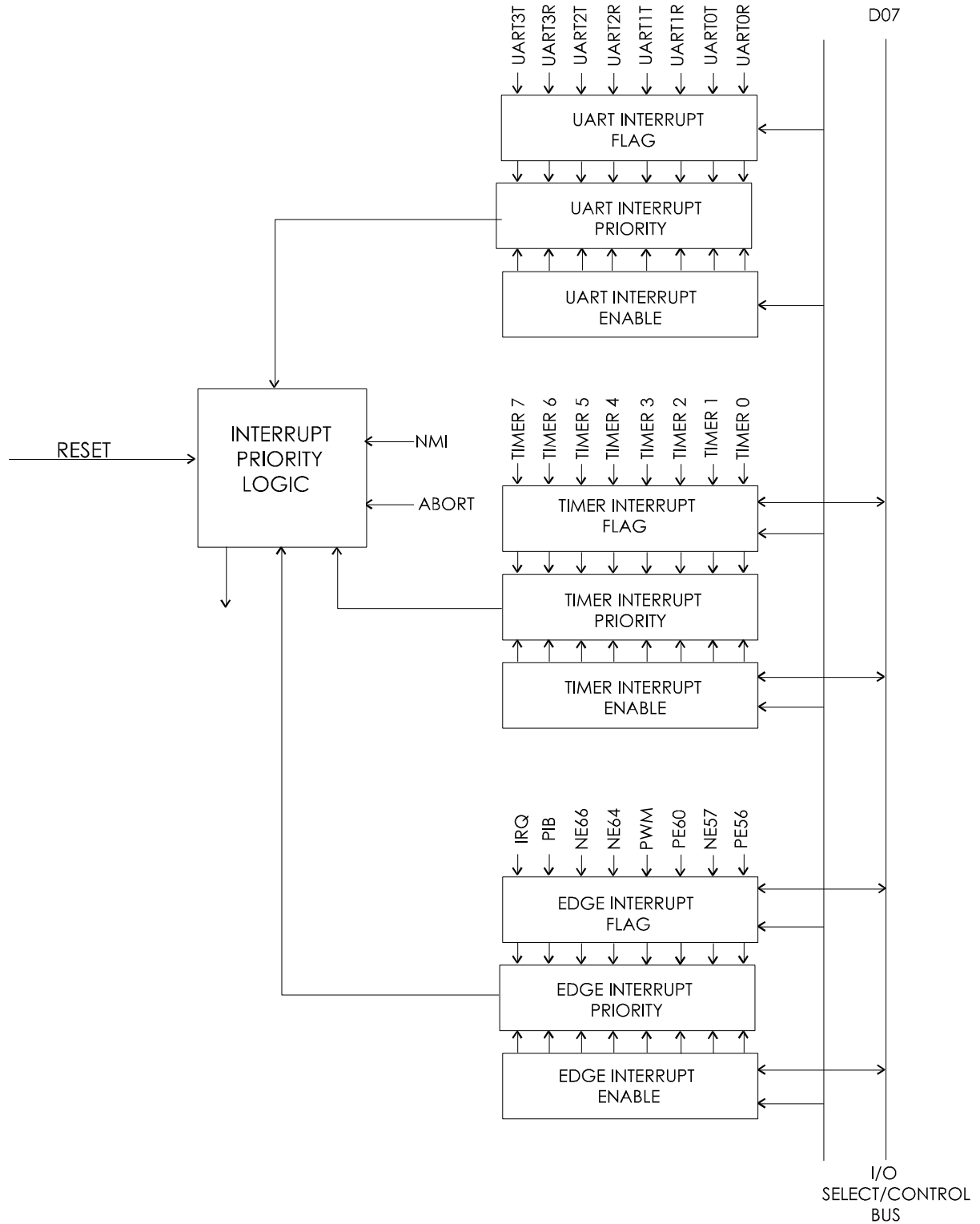
Figure 5-1 Interrupt Controller Block Diagram
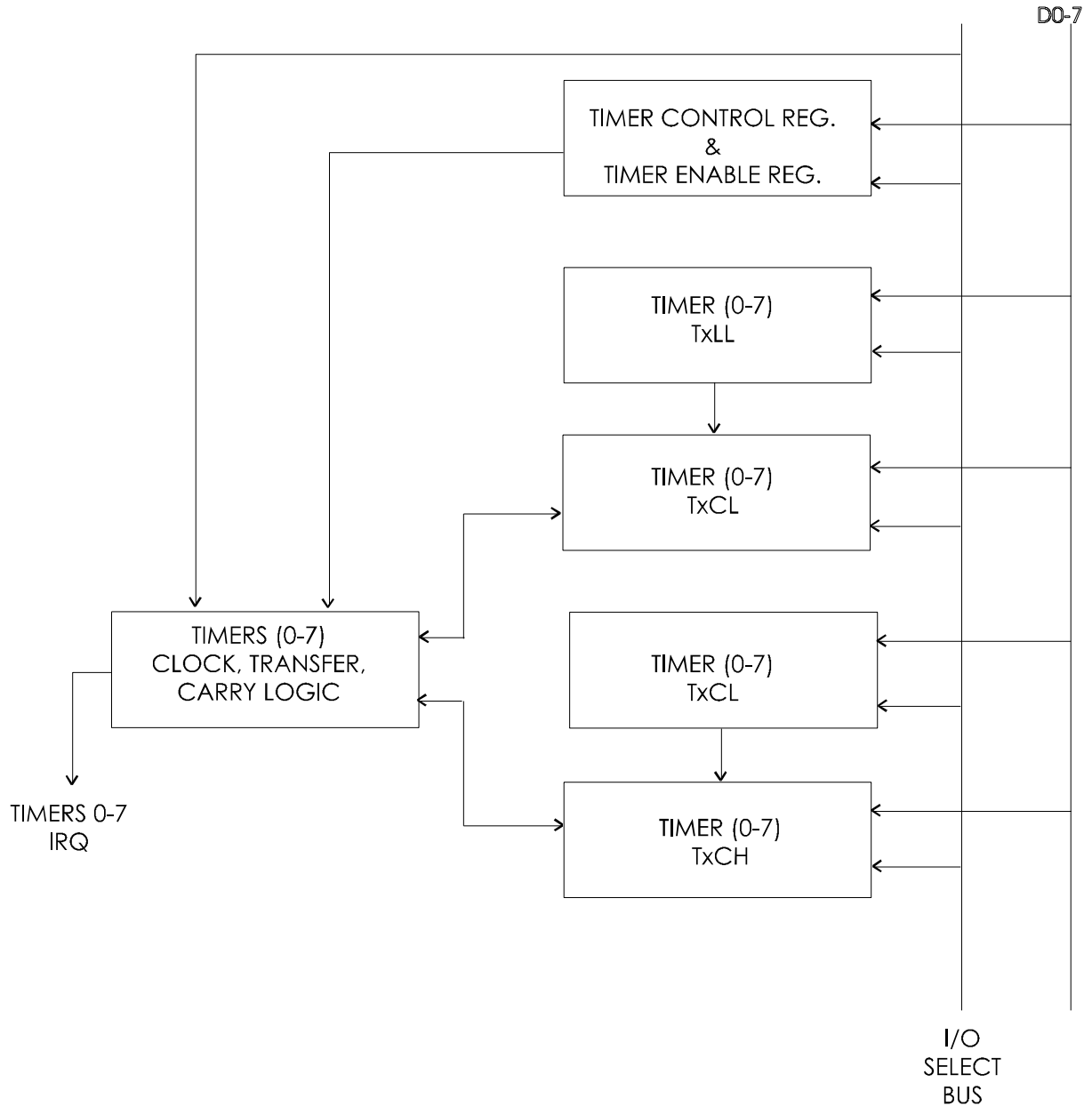
Figure 5-2 Timers 0-7 Block Diagram
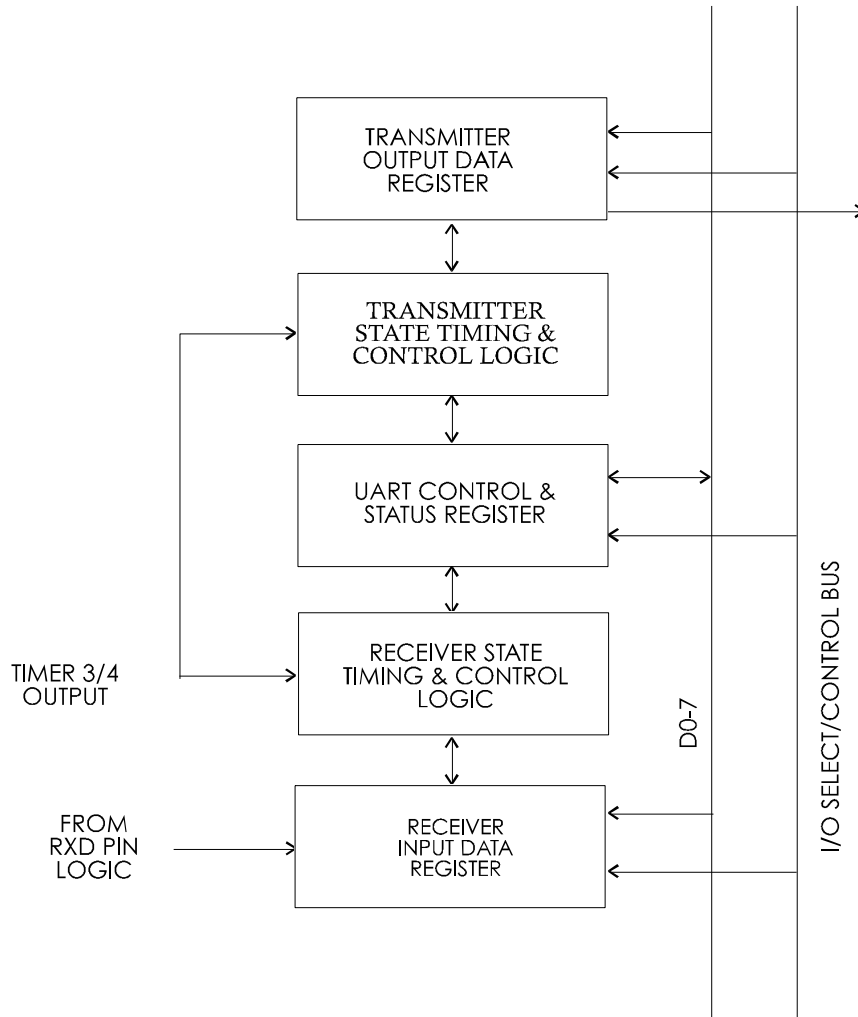
Figure 5-3 UART Block Diagram
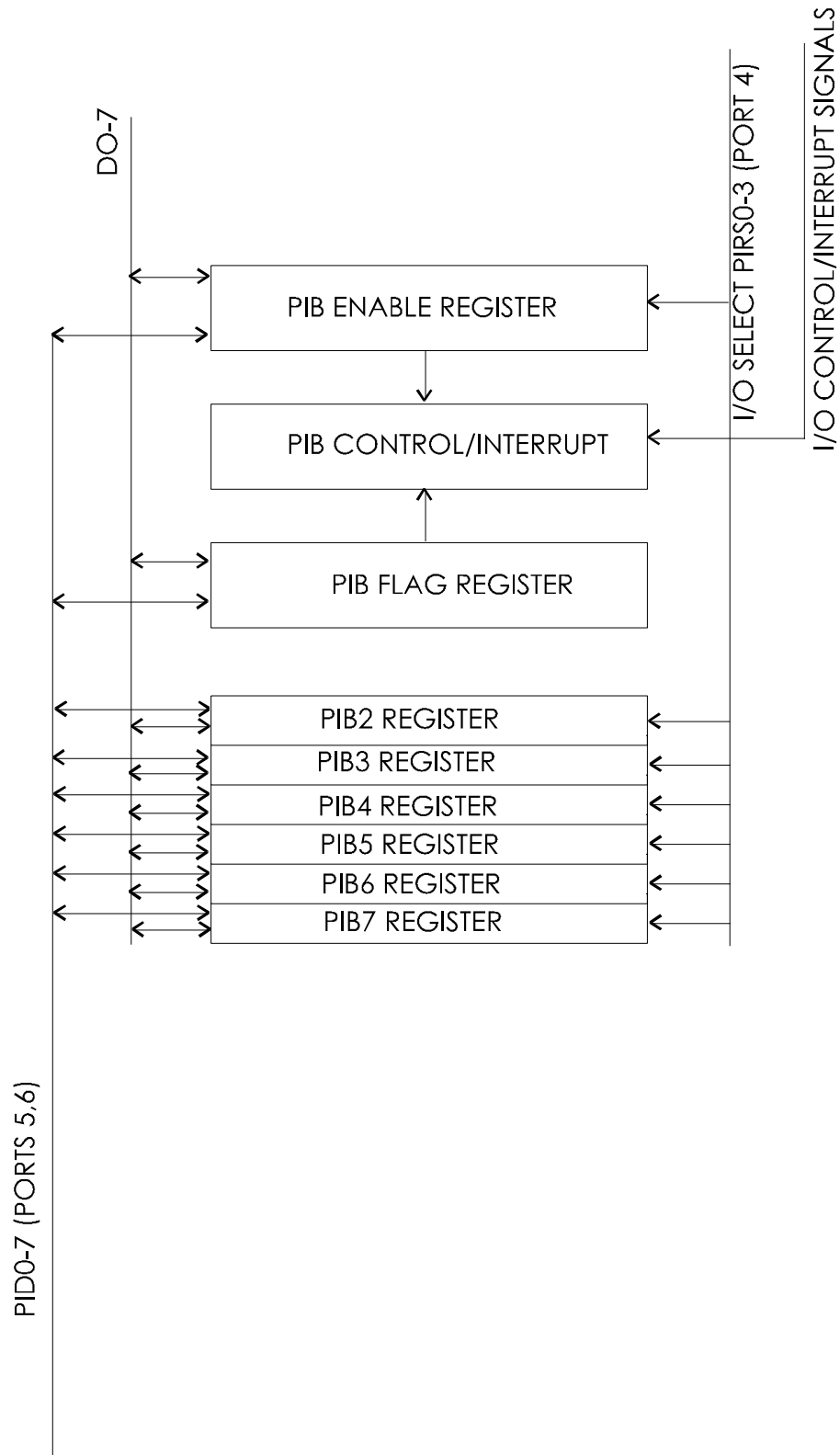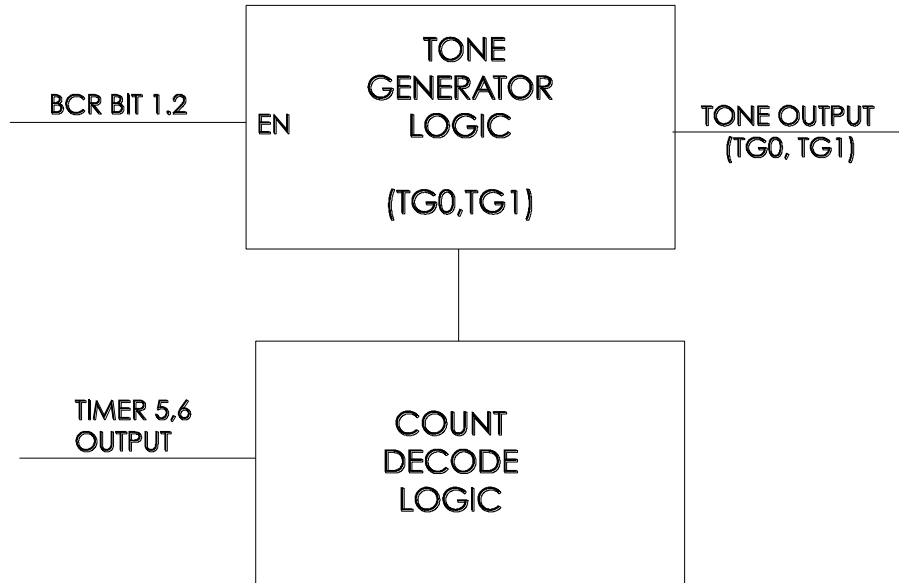
Figure 5-4 PIB Block Diagram

Figure 5-6 Tone Generator (TGx) Block Diagram

5.1 Recommended CLK and FCLK oscillators

The following circuit is a possible clocking system for the W65C265S providing both 32.768 KHz and 4 MHz frequencies. The 32.768 KHz clock is well suited for setting up a time of day clock with one of the W65C265S's internal timers.

In constructing this oscillator circuit, components should be kept as physically close to the W65C265S as possible and any excess in component leads should be trimmed off.
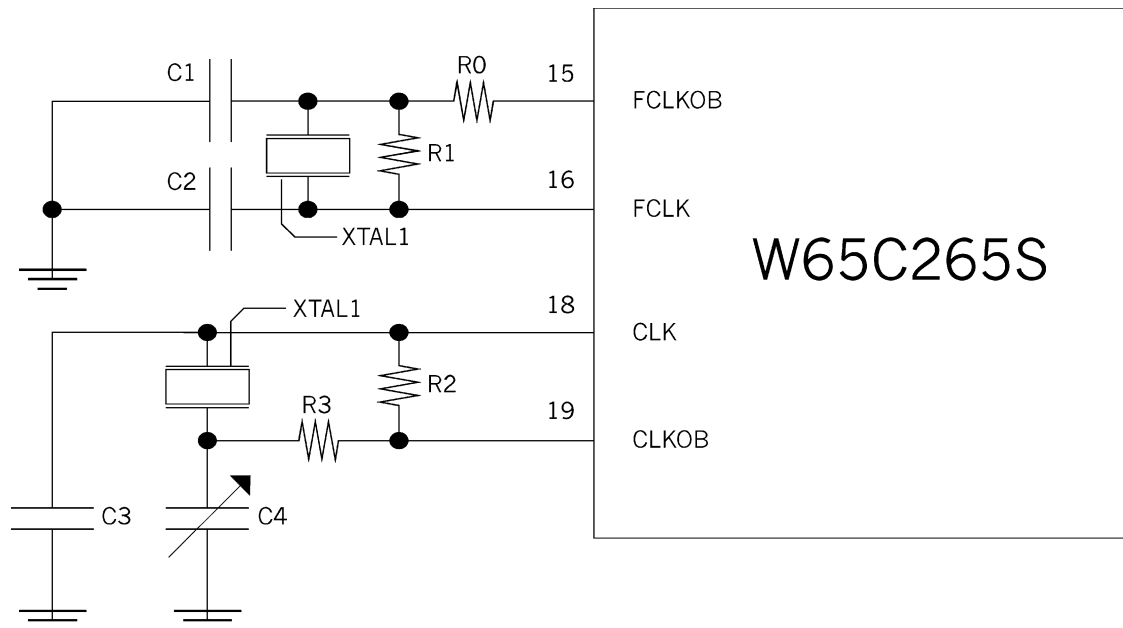
C1 = 47pF   R0 = 100Ω
C2 = 27pF   R1 = 800KΩ
C3 = 22pF   R2 = 2.6MΩ
C4 = 5-30pF variable   R3 = 150KΩ
XTAL1 = 4 MHz   XTA L2 = 32.768 KHz

Figure 5.1-1 Oscillator Circuit

Note:

1. Depending on trace layout or construction techniques used, values may need to be altered slightly.
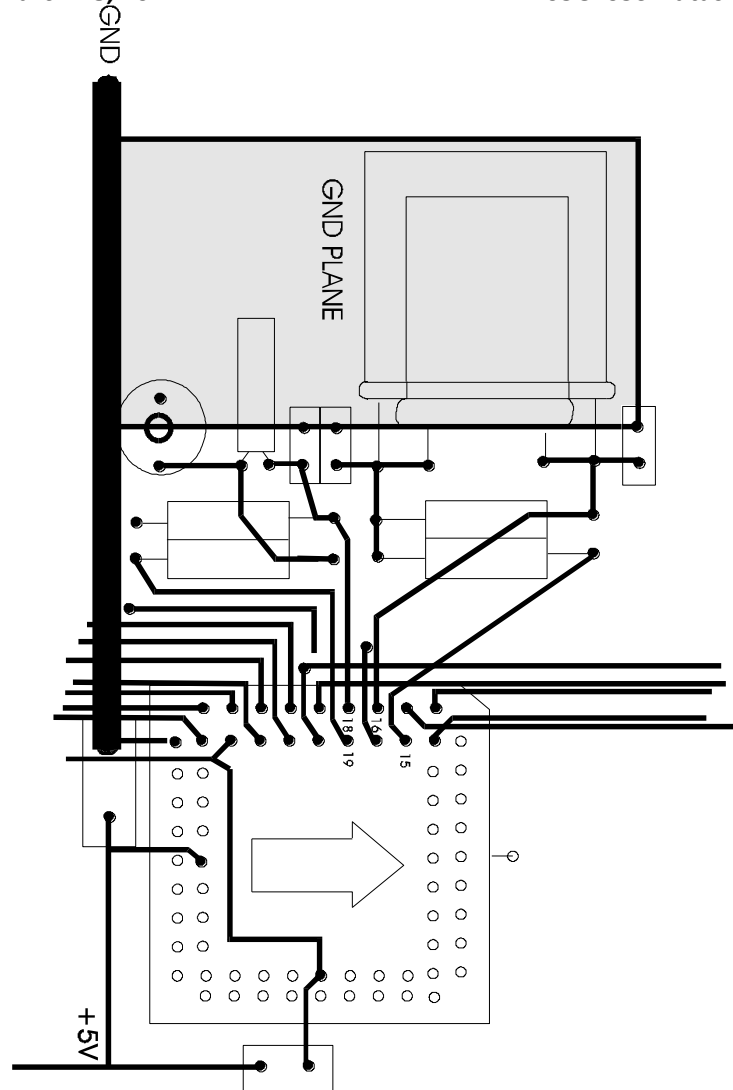2. Pin numbers only apply to PLCC package only.

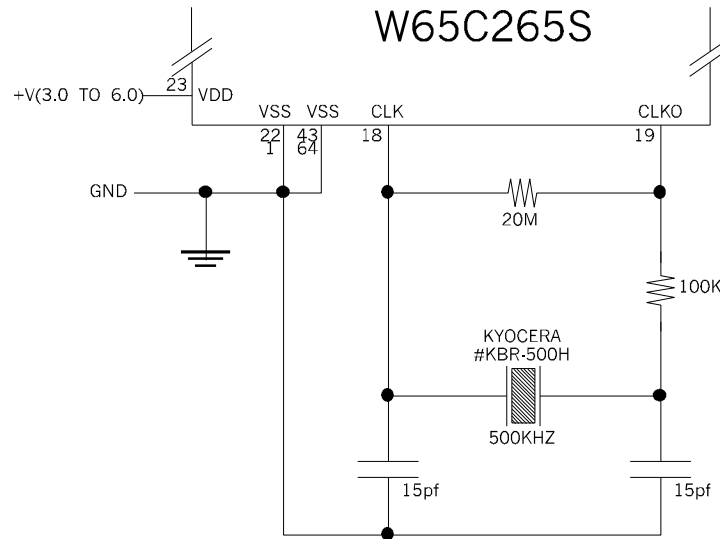**Figure 5.1-2 Circuit Board Layout for Oscillator Circuit**

Figure 5.1-3 Resonator Circuit

5.2 Wait state information and uses for the BE pin

The BE pin has two functions; allowing DMA into the W65C265S (BE function) and stopping the microprocessor (RDY function). Changing BE during PHI2 low time changes the BE function; changing BE during PHI2 high time changes RDY. If you want to stop the processor, you should pull BE low in the PHI2 high time for as many cycles as needed. Pulling the BE low in PHI2 high time does not tri-state the memory bus. Note also that the PHI2 pin does not stay high while RDY is pulled low; PHI2 going out will continue normally regardless of BE.

Pulling BE low during PHI2 low time turns off the output buffers on the address pins; however, the pins do not float because of weak bus holding devices. Note that the addresses are really inputs to the W65C265S when BE is low. If an external driver puts an address on the bus while BE is low, internal memory (RAM, ROM, or memory-mapped registers) will be accessed depending on the state of WEB. If you have no desire to turn off the busses when you slow down for the peripheral chips, you should hold BE high while you hold RDY low. That is,

BE = (PHI2BAR or RDY)

Where PHI2BAR is PHI2 inverted and delayed at least 10ns. RDY is your signal to request the microprocessor to stop. If you are not using the FCLK oscillator, another (less desirable) way to stop the microprocessor is to extend the low or high time of FCLK as long as you need to. This will work only if you know the microprocessor is using FCLK, not CLK.

6 ORDERING INFORMATION

W65C265S8QG-8	
Description W65C = standard product	W65C
Product Identification Number	265S
Foundry Process 8 = .8u	8
Package PL = Plastic Leaded Chip Carrier, 84 pins Q = Quad Flat Pack, 100 pins	Q
RoHS/Green Compliance G = RoHS/Green Compliant (Wafer and Packaging)	G
Temperature/Processing Blank = 0˚C to +70˚C	
Speed Designator -8 = 8MHz	-8

To receive general sales or technical support on standard product or information about our module library licenses, contact us at:

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Mesa, Arizona 85213 USA
Phone: 480-962-4545   Fax: 480-835-6442
Info@WesternDesignCenter.com
www.WDC65xx.com

WARNING: MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly when repair.